cPCI-9116

64 Ch, 16 bit, 250KS/s
Analog input Card
For 3U CompactPCI
User's Guide

Recycled Paper

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Product Model	
Environment to Use	☐ OS_____ ☐ Computer Brand_____ ☐ M/B: ☐ CPU: ☐ Chipset: ☐ BIOS: ☐ Video Card: ☐ Network Interface Card: ☐ Other:
Challenge Description	
Suggestions for ADLINK	

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How to Use This Guide

This manual is designed to help you use the cPCI-9116. The manual describes how to modify various settings on the cPCI-9116 card to meet your requirements. It is divided into seven chapters:

- **Chapter 1,** "Introduction", gives an overview of the product features, applications, and specifications.
- **Chapter 2,** "Installation", describes how to install the cPCI-9116. The layout of cPCI-9116 is shown.
- **Chapter 3,** "Signal Connection", describes the connectors' pin assignment and how to connect the outside signal and devices with the cPCI-9116.
- **Chapter 4,** "Registers Structure & Format", describes the details of register format and structure of the cPCI-9116. This information is important for the programmers who want to control the hardware by low-level programming.
- **Chapter 5,** "Operation Theorem", describes how to operate the cPCI-9116. The A/D, DIO and timer/counter functions are introduced. Also, some programming concepts are specified.
- **Chapter 6,** "Software Utility & Calibration", describes how to run the utility program included in the software CD and how to calibrate the cPCI-9116 for accurate measurement.

1

Introduction

The cPCI-9116 series is an advanced data acquisition card based on the 32-bit CompactPCI architecture. High performance designs and the state-of-the-art technology make this card ideal for data logging and signal analysis applications in medical, process control, and etc.

1.1 Features

The cPCI-9116 CompactPCI Advanced Data Acquisition Card provides the following advanced features:

- 32-bit PCI-Bus, plug and play
- Up to 64 single-ended inputs or 32 differential inputs , mixing of using SE and DI analog signal sources
- 16-bit analog input resolution
- On-board A/D 1K FIFO memory
- 512 analog input Channel Gain Queue spaces
- Sampling rate up to 250KS/s
- Bipolar or Unipolar input signals
- Programmable gain of x1, x2, x4, x8
- Jumperless and software configurable
- Five A/D trigger modes: software trigger, pre-trigger, post-trigger, middle-trigger and delay-trigger
- Software Polling, Interrupt and Bus-mastering DMA data transfer available
- 8 digital input and 8 digital output channels
- Compact size : standard compact PCI 3U size

1.2 Applications

- Automotive Testing
- Cable Testing
- Trancient signal measurement
- ATE
- Laboratory Automation
- Biotech measurement

1.3 Specifications

- **Analog Input (A/D)**
  - **Converter** :

    LT1606 (or equivalent) 250KHz
  - **Number of channels : (programmable)**

    64 single-ended(SE)

    32 differential input(DI)

    Mixing of using SE and DI analog signal sources
  - **A/D Data FIFO Buffer Size :** 1024 locations
  - **Channel Gain Queue Length :** 512 configurations
  - **Resolution :** 16-bit
  - **Input Range :** (Controlled by Channel Gain Queue)

    Bipolar : ± 5V, ±2.5V, ±1.25V, ±0.625V

    Unipolar: 0~10V, 0~5V, 0~2.5V, 0~1.25
  - **Overvoltage Protection :** Continuous ± 35V maximum
  - **Accuracy :** 0.01% of FSR
  - **Input Impedance :** 100 MΩ | 6pF
  - **Time-base source :** Internal 24MHz or

    External clock Input (fmax:24MHz, fmin: 1MHz)
  - **Programmable scan interval and sampling rate (divided from time-base source)**
  - **Trigger Mode :** Software-trigger, Pre-trigger, Post-trigger, Middle-Trigger, and Delay Trigger
  - **Data Transfer :** polling, EOC interrupt transfer, FIFO half-full interrupt transfer, and bus-mastering DMA
  - **Data Throughput :** 250KHz (maximum)

- **Digital I/O (DIO)**

- **Channel :** TTL compatible 8 digital inputs and 8 digital outputs
- **Input Voltage :**

  Low : VIL=0.8 V max.; IIL=0.2mA max.

  High : VIH=2.0V max.; IIH=0.02mA max
- **Output Voltage :**

  Low : VOL=0.5 V max.; IOL=8mA max.

  High : VOH=2.7V min; IOH=400μA

♦ **General Purpose Timer/ Counter**

- **Number of channel :** One 16-bit Up/Down Timer/Counter
- **Clock Input :** Internal 24MHz or External CLK input up to 20MHz

♦ **General Specifications**

- **Connector :** 100-pin D-type SCSI-II connector
- **Operating Temperature :** 0° C ~ 60° C
- **Storage Temperature :** -20° C ~ 80° C
- **humidity :** 5 ~ 95%, non-condensing
- **Power Consumption :** +5V @ 560mA typical

  +3.3V@ 100mA typical
- ±**15V (pin35, pin85) Output Current (max) :** 5mA
- **+5V(pin49, pin99) Output Current (max) :** 500mA
- **Dimension :** Standard Compact PCI 3U size

1.4 Software Support

ADLINK provides versatile software drivers and packages for users' different approach to built-up a system. We not only provide programming library such as DLL for many Windows systems, but also provide drivers for other software package such as LabVIEW®.

All the software options are included in the ADLINK CD. The non-free software drivers are protected with serial licensed code. Without the software serial number, you can still install them and run the demo version for two hours for demonstration purpose. Please contact with your dealer to purchase the formal license serial code.

1.4.1 Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

- **PCIS-DASK** : Include device drivers and DLL for **Windows 98**, **Windows NT** and **Windows 2000**. DLL is binary compatible across Windows 98, Windows NT and Windows 2000. That means all applications developed with PCIS-DASK are compatible across Windows 98, Windows NT and Windows 2000. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of PCIS-DASK are in the CD. (\\Manual_PDF\Software\PCIS-DASK)

- **PCIS-DASK/X :** Include device drivers and shared library for Linux. The developing environment can be Gnu C/C++ or any programming language that allows linking to a shared library. The user's guide and function reference manual of PCIS-DASK/X are in the CD. (\Manual_PDF\Software\PCIS-DASK-X.)

The above software drivers are shipped with the board. Please refer to the "***Software Installation Guide***" in the package to install these drivers.

1.4.2 PCIS-LVIEW: LabVIEW® Driver

PCIS-LVIEW contains the VIs, which are used to interface with NI's LabVIEW® software package. The PCIS-LVIEW supports Windows 98/NT/2000. The LabVIEW® drivers are free shipped with the board. You can install and use them without license. For detail information about PCIS-LVIEW, please refer to the user's guide in the CD.

(\\Manual_PDF\Software\PCIS-LVIEW)

1.4.3 DAQBench™: ActiveX Controls

We suggest the customers who are familiar with ActiveX controls and VB/VC++ programming use the DAQBench™ ActiveX Control components library for developing applications. The DAQBench™ is designed under Windows 98/NT/2000. For more detailed information about DAQBench, please refer to the user's guide in the CD.

(\\Manual_PDF\Software\DAQBench\DAQBench Manual.PDF)

2

Installation

This chapter describes how to install the cPCI-9116. At first, the contents in the package and unpacking information that you should be careful of are described.

The cPCI-9116 performs an automatic configuration of the IRQ, port address, and BIOS address. You do not need to set those configurations as you use ISA form factor DAS card. Automatic configuration will let your system more reliable and safe when your system is running.

2.1 What You Have

In addition to this *User's Guide*, the package includes the following items:

- cPCI-9116 Analog input Data Acquisition Card
- ADLINK All-in-one Compact Disc
- Software Installation Guide

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2 Unpacking

Your cPCI-9116 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card module carton for obvious damage. Shipping and handling may cause damage to your module. Be sure there are no shipping and handling damages on the module before processing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note : DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAMAGED.

You are now ready to install your cPCI-9116.

2.3 cPCI-9116 Layout

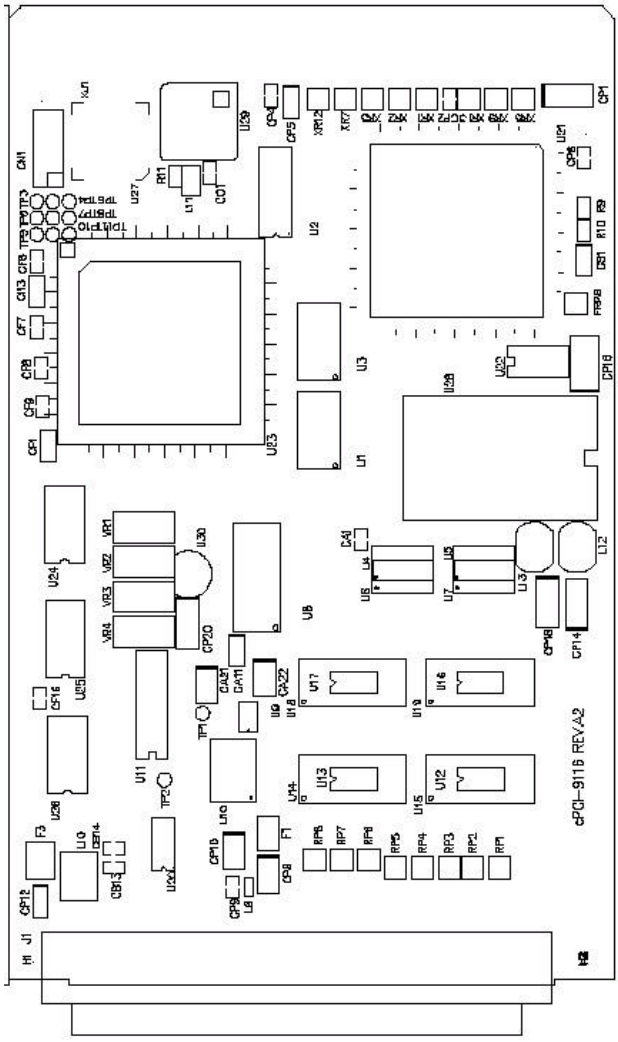


Figure 2.1 PCB Layout of the cPCI-9116

2.4 PCI Configuration

1. Plug and Play :

As a plug and play component, the board requests an interrupt number via a system call. The system BIOS responds with an interrupt assignment based on the board information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

2. Configuration :

The board configuration is done on a board-by-board basis for all PCI form factor boards on your system. Because configuration is controlled by the system and software, so there is no jumpers for base-address, DMA, and interrupt IRQ need to be set by the user.

The configuration is subject to change with every boot of the system as new boards are added or boards are removed. So, there is no idea what's going on to be installed.

3. Trouble shooting :

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it's likely caused by an interrupt conflict (perhaps because you incorrectly configured BIOS setup). In general, the solution, once you determine it is not a simple oversight, is to consult the BIOS documentation that come with your system.

3

Signal Connections

This chapter describes the connector of the cPCI-9116, and the signal connection between the cPCI-9116 and external devices.

3.1 Connectors Pin Assignment

The cPCI-9116 is equipped with one 100-pin SCSI-type connector, J1.

J1 is used for digital signal input, digital signal output, analog input, and timer/counter's signals. The pin assignment for the connector are illustrated in the Figure 3.1.

J1: Analog Input & Counter/Timer Digital Signal Input/Output.

	U_CMMD	1	51	AGND	
AIH0	AI0	2	52	AI32	AIL0
AIH1	AI1	3	53	AI33	AIL1
AIH2	AI2	4	54	AI34	AIL2
AIH3	AI3	5	55	AI35	AIL3
AIH4	AI4	6	56	AI36	AIL4
AIH5	AI5	7	57	AI37	AIL5
AIH6	AI6	8	58	AI38	AIL6
AIH7	AI7	9	59	AI39	AIL7
AIH8	AI8	10	60	AI40	AIL8
AIH9	AI9	11	61	AI41	AIL9
AIH10	AI10	12	62	AI42	AIL10
AIH11	AI11	13	63	AI43	AIL11
AIH12	AI12	14	64	AI44	AIL12
AIH13	AI13	15	65	AI45	AIL13
AIH14	AI14	16	66	AI46	AIL14
AIH15	AI15	17	67	AI47	AIL15
AIH16	AI16	18	68	AI48	AIL16
AIH17	AI17	19	69	AI49	AIL17
AIH18	AI18	20	70	AI50	AIL18
AIH19	AI19	21	71	AI51	AIL19
AIH20	AI20	22	72	AI52	AIL20
AIH21	AI21	23	73	AI53	AIL21
AIH22	AI22	24	74	AI54	AIL22
AIH23	AI23	25	75	AI55	AIL23
AIH24	AI24	26	76	AI56	AIL24
AIH25	AI25	27	77	AI57	AIL25
AIH26	AI26	28	78	AI58	AIL26
AIH27	AI27	29	79	AI59	AIL27
AIH28	AI28	30	80	AI60	AIL28
AIH29	AI29	31	81	AI61	AIL29
AIH30	AI30	32	82	AI62	AIL30
AIH31	AI31	33	83	AI63	AIL31
	AGND	34	84	AGND	
	+15V out	35	85	-15V out	
	N/C	36	86	N/C	
	DI0	37	87	DO0	
	DI1	38	88	DO1	
	DI2	39	89	DO2	
	DI3	40	90	DO3	
	DI4	41	91	DO4	
	DI5	42	92	DO5	
	DI6	43	93	DO6	
	DI7	44	94	DO7	
	ExtTimeBase	45	95	N/C	
	ExtTrg	46	96	GP_TC_CLK	
	SSH_OUT	47	97	GP_TC_GATE	
	GP_TC_OUT	48	98	GP_TC_UPDN	
	+5V out	49	99	+5V out	
	DGND	50	100	DGND	

Figure 3.1 Pin Assignment of J1

Legend :

U_CMMD	: User Common Mode
AIn	: Analog Input Channel n (single-ended)
AIHn	: Analog High Input Channel n (differential)
AILn	: Analog Low Input Channel n (differential)
DIn	: Digital Input Signal Channel n
DOn	: Digital Output Signal Channel n
ExtTimeBase	: External Timebase Clock Input
ExtTrg	: External Digital Trigger Signal
SSH_OUT	: SSH Output Signal
GP_TC_CLK	: General Purpose Timer/Counter Clock Input
GP_TC_GATE	: General Purpose Timer/Counter Gate Input
GP_TC_UPDN	:General Purpose Timer/Counter Up/Down Control Input (0:down, 1:up)
GP_TC_OUT	: General Purpose Timer/Counter Output
+5V OUT	: +5V Output
+15V OUT	: +15V Output
-15V OUT	: -15V Output
AGND	: Analog Ground
DGND	: Digital Ground
N/C	: No Connection

3.2 Analog Input Signal Connection

The cPCI-9116 provides up to 64 single-ended or 32 differential analog input channels. You could fill the Channel Gain Queue to get desired combination of the input signal types. The analog signal can be converted to digital value by the A/D converter. To avoid ground loops and get more accurate measurement of A/D conversion, it is quite important to understand the signal source type and how to choose the analog input modes : Single-ended, Differential, and User Common Mode.

3.2.1 Types of signal sources

Floating Signal Sources

A floating signal source means it is not connected in any way to the building ground system. A device with an isolated output is a floating signal source, such as optical isolator output, transformer output, and thermocouples.

Ground-Referenced Signal Sources

A ground-referenced signal means it is connected in some way to the building system. That is, the signal source is already connected to a common ground point with respect to the cPCI-9116, assuming that the computer is plugged into the same power system. Non-isolated outputs of instruments and devices which plug into the building power system are ground-referenced signal sources.

3.2.2 Input Configurations

Single-ended Mode

In the single-ended mode, all the input signals are connected to the ground provided by cPCI-9116. It is suitable for the connections with floating signal sources. Figure 3.2 shows the single-ended connection. Note that when more than two floating sources are connected, these sources will be referenced to the same common ground.

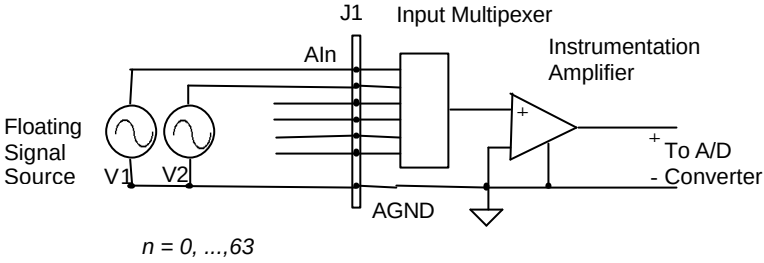


Figure 3.2 Floating source and single-ended

Differential input mode

The differential input mode provides two inputs that respond to the signal voltage difference between them. If the signal source is ground-referenced, the differential mode can be used for the common-mode noise rejection. Figure 3.3 shows the connection of ground-referenced signal sources under the differential input mode.

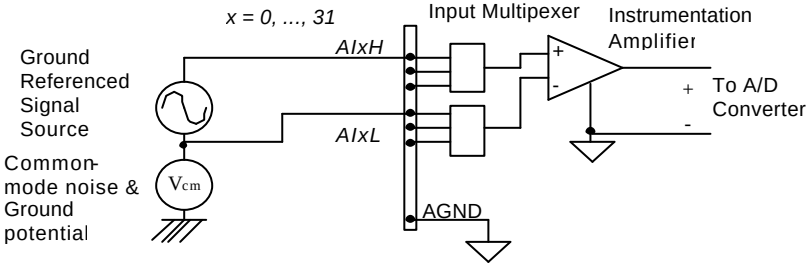


Figure 3.3 Ground-referenced source and differential input

Fig3.4 shows how to connect a floating signal source to cPCI-9116 in differential input mode. For floating signal sources, you need to add a resistor at each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100ohms, you can simply connect the negative side of the signal to AGND as well as the negative input of the Instrumentation Amplifier, without any resistors at all. In differential input mode, less noise couples into the signal connections than in single-ended mode.

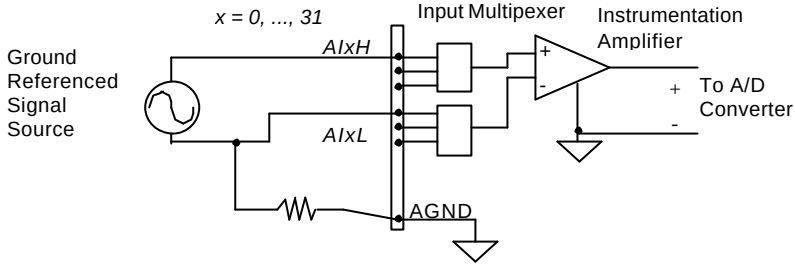


Figure 3.4 Floating source and differential input

User Common Mode(U_CMMD)

To measure ground-referenced signal sources which are connected to the same ground point, you could connect the signals in User-Common-Mode(U_CMMD). Fig3.5 illustrates the connections. The signal local ground reference is connected to the negative input of the instrumentation Amplifier, and the common-mode ground potential between signal ground and cPCI-9116 ground will be rejected by the instrumentation amplifier.

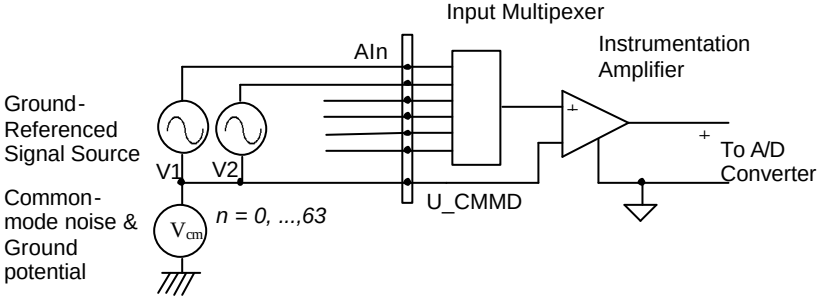


Figure 3.5

Ground-referenced source and User Common Mode connections

3.3 Digital I/O Connection

The cPCI-9116 provides 8 digital input and 8 digital output channels on board. The digital I/O signal are fully TTL/DTL compatible. The detailed digital I/O signal specification can be referred in section 1.3.

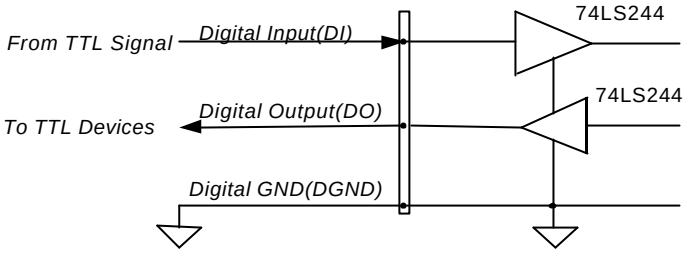


Figure 3.6 Digital I/O Connection

4

Registers Format

The detailed descriptions of the register format and structure of the cPCI-9116 are specified in this chapter. The information is quite useful for the programmers who wish to handle the card by low-level programming.

In addition, the low level programming syntax is introduced. The information can help the beginners to operate the cPCI-9116 in the shortest learning time.

4.1 I/O Port Address

The cPCI-9116 functions as 32-bit PCI master device to any master on the PCI bus. It supports burst transfer to memory space by using 32-bit data. All data reads and writes are based on 32-bit transactions. The Table 4.1 shows the I/O address of each register with respect to the base address. The function of each register are also shown.

I/O Address	Read	Write
Base + 0x00	Scan Interval Counter	Scan Interval Counter
Base + 0x04	Sample Interval Counter	Sample Interval Counter
Base + 0x08	Scan Counter	Scan Counter
Base + 0x0C	DIV Counter	DIV Counter
Base + 0x10	Delay1 Counter	Delay1 Counter
Base + 0x14	M Counter	M Counter
Base + 0x18	GP Counter/Timer 0	GP Counter/Timer 0
Base + 0x1C	X	X
Base + 0x20	X	GP Counter/Timer Control Reg
Base + 0x24	A/D FIFO Data Reg	Config. Channel Gain Queue Reg..
Base + 0x28	A/D and FIFO Status Reg.	A/D and FIFO Control Reg.
Base + 0x2C	X	X
Base + 0x30	Digital IN Reg.(Dout)	Digital OUT Reg.
Base + 0x34	X	A/D Trigger Mode Reg.
Base + 0x38	Interrupt Reason Reg.	Interrupt Control Reg.

Table 4.1 I/O Address

4.2 Internal Timer/Counter Register

In cPCI-9116, basically there are 6 counters which are responsible for the scan timing of the analog input data acquisition. The 6 counters occupies 6 I/O address locations in the cPCI-9116 as shown blow.

Address : BASE + 0 ~ BASE + 14

Attribute : read / write

Data Format :

Base + 0x00	Scan Interval Counter Register (R/W) 24bit
Base + 0x04	Sample Interval Counter Register (R/W) 16bit
Base + 0x08	Scan Counter Register (R/W) 24bit
Base + 0x0C	DIV Counter Register (R/W) 9bit
Base + 0x10	Delay1 Counter Register (R/W) 16bit
Base + 0x14	M ounter Register (R/W) 16bit

SI_counter : Scan Interval counter

SI2_counter : Sample Interval counter

SC_counter : total Scan Count counter

DIV_counter : specify the number of samples per scan

DLY1_counter : Delay Interval counter (only used in delay trigger mode)

M_counter : specify the number of scans before a trigger (only used in pre-trigger and middle-trigger modes)

4.3 General Purpose Timer/Counter Register

One 16-bit, general-purpose timer/counter exists in the cPCI-9116. Writing to this register loads the initial count value into the general-purpose timer/counter. Reading from this register feedbacks the current count value of the general-purpose timer/counter

Address : BASE + 0x18

Attribute : write / read

Data Format :

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

4.4 General Purpose Timer/Counter Control Register

Address : BASE + 0x20

Attribute : write only

Data Format :

Bit	7	6	5	4	3	2	1	0
	Counter en	Up Down	Up Down src	Gate_src	Clk_src	---	MODE1	MODE0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
		---	---	---	---	---	---	---
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	**---**	**---**	**---**	**---**	**---**	**---**	**---**

Counter en (bit7) : GPTC0 count enable

1: enable GPTC0

0: disable GPTC0

UpDown (bit6) : GPTC0's up/down pin software control

1: Up counter

0: Down counter

UpDown src(bit5) : GPTC0's up/down pin selection bit

1: External input (Pin 98)

0: Software Control

Gate_src (bit4) : GPTC0's gate source

1: External Input (Pin 97)

0: gate controlled by setting the enable (bit7)

Clk_src (bit3) : GPTC0's clock source

1: External Input (Pin 96)

0: Internal Timebase

MODE1~MODE0 (bit1 ~ bit0) : GPTC0's Mode selection

MODE1	MODE0	Description
0	0	General Counter
0	1	Pulse Generation
1	0	X
1	1	X

4.5 A/D Data Registers

The digital data converted from cPCI-9116 will be stored in the A/D data registers. The 16 bit A/D-data is put into 32-bit registers.

Address : BASE +24

Attribute : read

Data Format :

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

AD15 .. AD0 :Analog to digital data. AD15 is the Most Significant Bit (MSB). AD0 is the Least Significant Bit (LSB).

4.6 Channel Gain Queue Register

This register is used to fill the Channel Gain Queue. We recommend users use our function call to avoid any possible errors from these settings.

Address : BASE + 0x24

Attribute : write

Data Format :

Bit	7	6	5	4	3	2	1	0
	EN3	EN2	EN1	EN0	HL_sel	UNIP	DIFF	U_CMMD
Bit	15	14	13	12	11	10	9	8
	---	---	Gain1	Gain0	CH3	CH2	CH1	CH0
Bit	23	22	21	20	19	18	17	16
	---	---	---	---	---	---	---	---
Bit	31	30	29	28	27	26	25	24
	---	---	---	---	---	---	---	---

CH3 ~ CH0 (bit11~ bit8) : Internal A/D Channel selection bits

EN3 ~ EN0 (bit7~ bit4) : Multiplexer Enable selection bits

Gain1~Gain0 (bit13~bit12) : Gain selection bits

Gain1	Gain0	Gain
0	0	1
0	1	2
1	0	4
1	1	8

HL_sel(bit3) : >31 channel selection (single ended)

1: when channel number is larger than 31

0: when channel number is smaller than or equal to 31

DIFF(bit1) : Analog Input Signals Type

1: Differential

0: Single ended

UNIP(bit2) : Analog Input Signals Polarity

1: Unipolar

0: Bipolar

U_CMMD (bit0): User Defined Common Mode Selection

1: User Defined Common Mode (Pin 1)

0: Local Ground of cPCI-9116

4.7 A/D & FIFO Control Register

Address : BASE + 28

Attribute : Write

Data Format :

Bit	7	6	5	4	3	2	1	0
	SC_dis	Clear Channel Gain Queue	Set done	Clear DFIFO	Clear Trg_det	Clear SC_TC	Clear ADOR	Clear ADOS
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	---	---	---	---	---	---	---	DMA
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

DMA (Bit8) : Write Only, set for DMA transfer

SC_dis (Bit7): Write Only, set to disable the SC counter

clear Channel Gain Queue (Bit6): Write Only

clear the Channel Gain Queue

0: no effect on the Channel Gain Queue

1: clear the Channel Gain Queue

set done (Bit5) : Write Only

0: indicate the Channel Gain Queue is not ready

1: indicate the Channel Gain Queue is OK

clear DFIFO(Bit4) : Write Only

clear the Data FIFO

0: no effect on Data FIFO

1: clear the Data FIFO

clear Trg_det(Bit3) : Write 1 to clear

write 1 to clear the trigger status

0: no effect

1: clear trigger detect status

clear SC_TC(Bit2) : Write 1 to clear

write 1 to clear Scan Counter Terminal Count status

0: no effect

1: clear the SC_TC status

clear ADOR(Bit1) : Write 1 to clear

write 1 to clear the A/D Overrun Status

0: no effect

1: clear the A/D Overrun status

clear ADOS(Bit0) : Write 1 to clear

write 1 to clear the A/D Over Speed Status

0: no effect

1: clear the A/D OverSpeed status

4.8 A/D & FIFO Status Register

Address : BASE + 28

Attribute : read

Data Format :

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	ACQ	Full	HFull	Empty	Trg_det	SC_TC	ADOR	ADOS
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	---	---	---	---	---	---	---	---
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

ACQ (Bit7) : Read Only, set when acquisition is in progress.

Full (Bit6) : Read Only

A/D FIFO Full status (Fatal Error !)

0: FIFO Full

1: FIFO not Full

HFull(Bit5): Read only

A/D FIFO Half Full status

0: FIFO Half Full

1: FIFO not Half Full

Empty (Bit4) : Read Only

A/D FIFO Empty status

0: FIFO Empty

1: FIFO not Empty

Trg_det (Bit3) : Read/ Write 1 to clear

External Digital Trigger Status

1: External Digital Trigger ever Happened

0 : No External Digital Trigger

SC_TC(Bit2) : Read/ Write 1 to clear

Scan Counter Terminal Count Status

1: Scan Counter counts to 0

0: Scan Counter not Completed

ADOR(Bit1) : Read/ Write 1 to clear

A/D Overrun Status (Fatal Error !)

1: A/D Overrun

0: A/D not Overrun

ADOS(Bit0) : Read/ Write 1 to clear

A/D Over Speed Status (Warning !)

1: A/D Over Speed

0: A/D not Over Speed

4.9 Digital I/O register

There are 8 digital input channels and 8 digital output channels provided by the cPCI-9116. The address Base + 30 is used to access digital inputs and control digital outputs.

Address : BASE +30

Attribute : read

Data Format :

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

Address : BASE + 30

Attribute : write

Data Format :

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	---	---	---	---	---	---	---	---
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

4.10 A/D Trigger Mode Register

Address : BASE + 0x34

Attribute : write only

Data Format :

Bit	7	6	5	4	3	2	1	0
	Retrig	DLYSRC	Time Base	TrgP	MODE2	MODE1	MODE0	---
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	---	---	---	---	---	softconv	ACQ_EN	M_enable
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

softconv (bit10) : ADC direct conversion control

1: generate 1 convert pulse

0: no effect

ACQ_EN (bit9) : Acquisition enable bit

1: enable the acquisition timing

0: disable the acquisition timing

M_enable (bit8) : M counter enable bit

1: ignore trigger signals before M counter reaches 0

0: accept the trigger signal anytime

Retrig (bit7) : Retriggerability in a acquisition

1: Retriggerable

0: trigger only once

DLY SRC (bit6) : Delay time unit in delay trigger mode

1: delay in sampling rate (SI2)

0: delay in Timebase

TimeBase(bit5) : The Timebase Selection of cPCI-9116

1: External Timebase

0: Internal Timebase (24 MHz)

TrgP (bit4) : The Trigger polarity selection bit

1: Negative Edge Trigger

0: Positive Edge Trigger

MODE2 ~ 0(bit3 ~ bit1) : Trigger Mode Selection Bits

MODE2	MODE1	MODE0	Description
0	0	0	Software Trigger
0	0	1	Post Trigger
0	1	0	Delay Trigger
0	1	1	Pre Trigger
1	0	0	Middle Trigger

4.11 Interrupt Control Register

Address : BASE + 0x38

Attribute : write

Data Format :

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	---	---	---	Clr_Timer	Clr_STTC	Clr_Hfull	Clr_DTrg	Clr_EOC
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	---	---	---	Timer_en	STTC_en	Hfull_en	DTrg_en	EOC_en
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

Timer_en (bit12) : General Purpose Timer Interrupt Enable Control

1: Enable

0: Disable

SCTC_en (bit11) : About Trigger Complete Interrupt Enable Control

1: Enable

0: Disable

Hfull_en (bit10) : A/D FIFO Half Full Interrupt Enable Control

1: Enable

0: Disable

DTrg_en (bit9) : External Digital Trigger Interrupt Enable Control

1: Enable

0: Disable

EOC_en (bit8) : End of conversion Interrupt Enable Control

1: Enable

0: Disable

Clr_Timer (bit4) : write 1 to clear the GPTC Interrupt status

1: clear interrupt from the GPTC

0: no effect

Clr_SCTC (bit3) : write 1 to clear the SCTC Interrupt

1: clear the interrupt on terminal count of the Scan counter

0: no effect

Clr_HFull (bit2) : write 1 to clear the data FIFO half full interrupt

1: clear the interrupt on the data FIFO half full status

0: no effect

Clr_DTrg (bit1) : write 1 to clear the Digital Trigger Interrupt

1: clear the interrupt when trigger happens

0: no effect

Clr_EOC (bit0) : write 1 to clear the End of conversion Interrupt

1: clear the interrup when EOC

0: no effect

4.12 Interrupt Status Register

Address : BASE + 0x38

Attribute : read

Data Format :

Bit	7	6	5	4	3	2	1	0
	---	---	---	Timer	STTC	Hfull	DTrg	EOC
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	---	---	---	---	---	---	---	---
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	---	---	---	---	---	---	---	---
Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
	---	---	---	---	---	---	---	---

Timer (bit4) : GPTC generated Interrupt status

1: Interrupt Occurs

0: Interrupt not Occur

SCTC(bit3) : Scan Counter reach Terminal Count Interrupt status

1: Interrupt Occurs

0: Interrupt not Occur

HFull (bit2) : data FIFO Half Full Interrupt

1: Interrupt Occurs

0: Interrupt not Occur

DTrg (bit1) : Digital Trigger Interrupt status

1: Interrupt Occur

0: Interrupt not Occur

EOC (bit0) : End of Conversion Interrupt status

1: Interrupt Occurs

0: Interrupt not Occur

5

Operation Theorem

The operation theorem of the functions on cPCI-9116 is described in this chapter. The functions include the A/D conversion, Digital I/O and General Purpose Counter / Timer. The operation theorem can help you understand how to manipulate and program the cPCI-9116.

5.1 A/D Conversion

5.1.1 A/D Conversion Procedure

When using an A/D converter, users should know about the properties of the signal to be measured at first. Users can decide which channel to use and connect the signals to the cPCI-9116. Please refer to 3.2. In addition, users should define and control the A/D signal configurations, including channels, gains, and A/D signal types.

The A/D acquisition is initiated by a trigger source, users must decide how to trigger the A/D conversion . The data acquisition will start when a trigger condition is met.

After the end of A/D conversion, the A/D data is buffered in a Data FIFO. The A/D data should be transferred into PC's memory for further processing.

Two of the acquisition modes: Software Polling and Scan acquisition are described separately in the following, including the timing, signal source control, trigger mode, and transfer method.

5.1.2 Software conversion with polling data transfer acquisition mode(Software Polling)

This is the easiest way to acquire a single A/D data. The A/D converter starts a conversion when the user writes 1 into the bit10 of the A/D trigger mode register (BASE+34). After the A/D conversion is initialized by software, the software should poll the FIFO ***Empty*** status (bit4) in the A/D & FIFO Status register (BASE+28) until it changes to low level.

If Data FIFO is empty before an A/D conversion starts, the ***Empty*** bit will be high. After the A/D conversion is completed, the A/D data is written to Data FIFO immediately, thus the ***Empty*** becomes low. You can consider the ***Empty*** bit as a flag to indicate the converted data ready status. That is, a low ***Empty*** bit means the data is ready. Then the A/D data could be transferred to host memory from FIFO.

This method is very suitable for the application that needs to process AD data in real time. Under this mode, the timing of the A/D conversion is fully controlled under software. However, it is difficult to control the fixed A/D conversion rate except another timer interrupt service routine is used to generate a fixed conversion rate trigger.

In our software driver, we provide an integral function to acquire a single data (That is , it will start an A/D conversion, then poll the ***Empty*** flag and read the data back when the data is ready) . We also provide an individual function to let user start an A/D conversion only, and then users must read it back from A/D data register (BASE+24) by themselves. This method makes it possible to read A/D converted data without polling. The conversion and acquisition time of the ADC in cPCI-9116 will not excess 4μs on cPCI-9116 card. Hence, after software conversion, the software can wait for at least 4μs then read the A/D Data Register without polling.

5.1.2.1 Specifying Channels, Gains, and input configurations in the Channel Gain Queue

In both the Software Polling and programmable scan acquisition mode, the channel, gain, and input configuration (single-end, differential, and U_CMMD) which you want to acquire samples can be specified in the **Channel Gain Queue**. You can fill the channel number in the Channel Gain Queue in any orders. Therefore, you can control the channel order for acquiring samples with different gain and input configuration for each channel. The maximum number of entries you can set is 512 channels. The channel order of acquisition is the same as the order you set in the Channel Gain Queue. When the specified channels are sampled from the first data to the last data in Channel Gain Queue, the channels in the Channel Gain Queue will be sampled again until the specified number of samples is acquired.

5.1.3 Programmable scan acquisition mode

5.1.3.1 Scan Timing and Procedure

It's recommended to use this mode if your applications need a fixed and precise A/D sampling rate. You can accurately program the period between conversions of individual channels in a scan and the period between conversions of the entire scan. There are at least 4 counters which need to be specified:

SI_counter(24 bit): Specify the **S**can **I**nterval = SI_counter / Timebase

SI2_counter(16 bit): Specify the data **S**ampling **I**nterval = SI2_counter/Timebase

SC_counter(24 bit): Specify **S**can **C**ount Counter after trigger

DIV_counter(9 bit): Specify the number of samples per scan

The acquisition timing and the meaning of the 4 counters is illustrated in figure 5.1.

Timebase clock source

In scan acquisition mode, all the A/D conversions start on the output of counters which use **Timebase** as the clock source. By software you can specify the Timebase to be either an internal clock source on board(24MHz) or an external clock input on pin45 of J1. The external clock is useful when you want to acquire data at rates not available with the internal A/D sample clock. The external clock source should generate TTL-compatibale continuous clocks, and the maximum frequency is 24MHz while the minimum is 1MHz.

3 Scans, 4 Samples per scan
(SC_Counter=3, DIV_Counter=4)

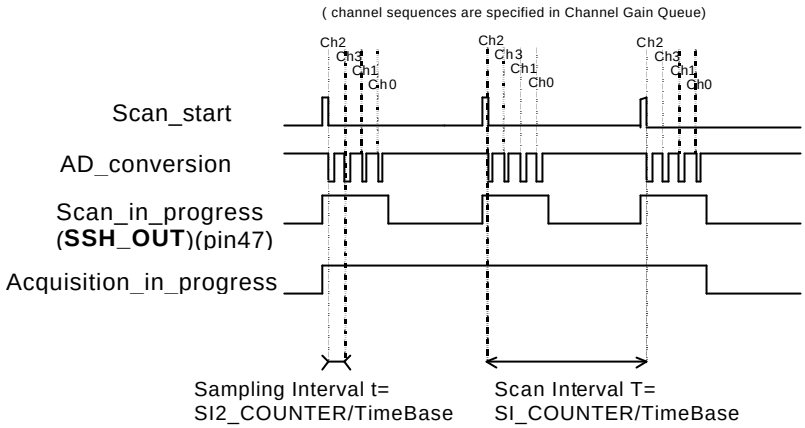


Figure 5.1 Scan Timing

In the scan acquisition mode, the channel, gains, and input configurations(single-end, differential, and U_CMMD) you want to acquire samples in a scan can be specified in a hardware **Channel Gain Queue**, please refer to 5.1.3.2 for the details.

There are 5 trigger modes to start the scan acquisition, please refer to 5.1.3.3 for the details. The data transfer modes were discussed in 5.1.3.4.

Note:

1. The maximum A/D sampling rate is 250kHz. Therefore, SI2_counter can't be smaller than 96 while using an internal Timebase.
2. The SI_counter is a 24 bit counter and the SI2_counter is a 16 bit counter. Therefore, the maximum scan interval while using an internal Timebase = 2^{24}/24M s = 0.699s, and the maximum sampling interval between 2 channels while using an internal Timebase = 2^{16}/24M s = 2.73ms.
3. The scan interval can't be smaller than the product of data sampling interval and the DIV_counter value. The relationship can be represented as : SI_counter>=SI2_counter*DIV_counter.

Scan with SSH

You can send the SSH_OUT signal on pin47 of J1 to an external S&H circuits to sample and hold all the signals if you want to simultaneously sample all channels in a scan, as illustrated in fig5.1.

Note: The 'SSH_OUT' signal is sent to external S&H circuits to hold the analog signal. Users must implement external S&H circuits on their own to carry out the S&H function. There are no on-board S&H circuits.

5.1.3.2 Specifying Channels, Gains, and input configurations in the Channel Gain Queue

Like software polling acquisition mode, the channel, gains, and input configurations(single-end, differential, and U_CMMD) you want to acquire samples in a scan can be specified in a hardware **Channel Gain Queue** under scan acquisition mode. Please refer to 5.1.2.1 for the details. Note that in scan acquisition mode the number of entries in the Channel Gain Queue is normally equivalent to the value of DIV_counter(that is, the numbers of samples per scan).

Example :

Set

SI2_counter = 240

SI_counter = 960

SC_counter = 3

DIV_counter = 4

Timebase = Internal clock source

Channel entries in the Channel Gain Queue : ch1, ch2, ch0, ch2

Then

Acquisition sequence of channels: 1, 2, 0, 2, 1, 2, 0, 2, 1, 2, 0, 2

Sampling Interval = 240/24M s = 10 us

Scan Interval = 960/24M s = 40 us

Equivalent sampling rate of ch0, ch1 : 25kHz

Equivalent sampling rate of ch2 : 50kHz

5.1.3.3 Trigger Modes

There are 5 trigger modes(software-trigger, pre-trigger, post-trigger, middle-trigger, and delay-trigger) to start the data acquisition described in 5.3.1.1. All but software trigger are external digital triggers. An external digital trigger event occurs when a rising edge or a falling edge (software programmable) of a digital signal is detected on pin46 of J1. They are described as follows.

Software-Trigger Acquisition

This trigger mode does not need any external trigger source. The data acquisition starts right after you execute the specified function calls to begin the operation. The scan timing is the same as fig5.1. The total acquired data length = DIV_counter*SC_counter.

Pre-Trigger Acquisition

Use pre-trigger acquisition in applications when you want to collect data before an external trigger event. The A/D starts when you execute the specified function calls to begin the operation, and it stops when the external trigger event occurs. Users must program the value M in **M_counter**(16bit) to specify the amount of stored scans of data before the trigger event. If the external trigger occurs after M scans of data are converted, the program only stores the last M scans of data, as illustrated in fig5.2, where M_counter = M =3, DIV_counter =4, SC_counter = 0. The total stored amount of data = DIV_counter *M_counter =12.

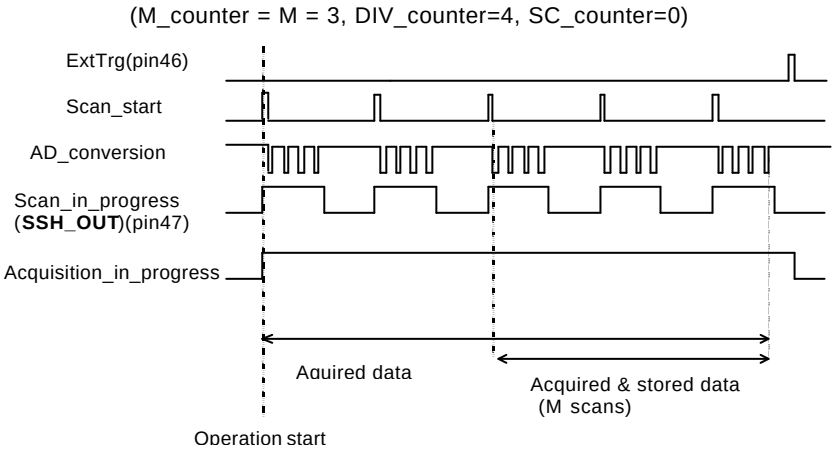


Figure 5.2 Pre-trigger(trigger occurs after M scans)

Note that If the external trigger event occurs when a scan is in progress, the data acquisition won't stop until this scan completes, and the stored M scans of data include the last scan. **Therefore, the first stored data will always be the first channel entry of a scan(that is, the first channel entry in the Channel Gain Queue** if the number of entries in the Channel Gain Queue is equivalent to the value of DIV_counter)**, no matter when the trigger signal occurs**, as illustrated in Fig5.3, where M_counter = M =3, DIV_counter = 4, SC_counter = 0.

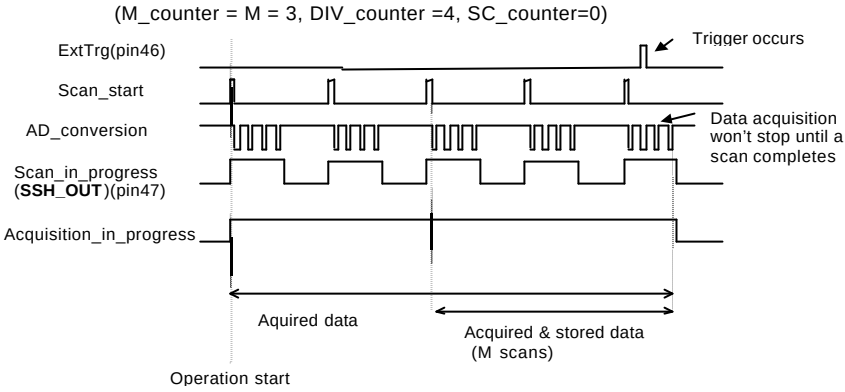


Figure 5.3 Pre-trigger(trigger occurs when a scan is in progress)

When the external trigger signal occurs before the first M scans of data are converted, the amount of stored data could be fewer than the originally specified amount DIV_counter * M_counter, as illustrated in fig 5.4. This situation can be avoided by setting **M_enable.** If **M_enable** is set to 1, the tigger signal will be ignored until the first M scans of data are converted, and It assures user can get M scans of data under pre-trigger mode, as illustrated in fig 5.5. However, if **M_enable** is set to 0, the trigger signal will be accepted in any time, as illustrated in fig 5.4. Note that the total amount of stored data is still always a multiple of DIV_counter (number of samples per scan) because the data acquisition won't stop until a scan complets.

(M_Counter = M = 3, DIV_Counter=4, SC_Counter=0)

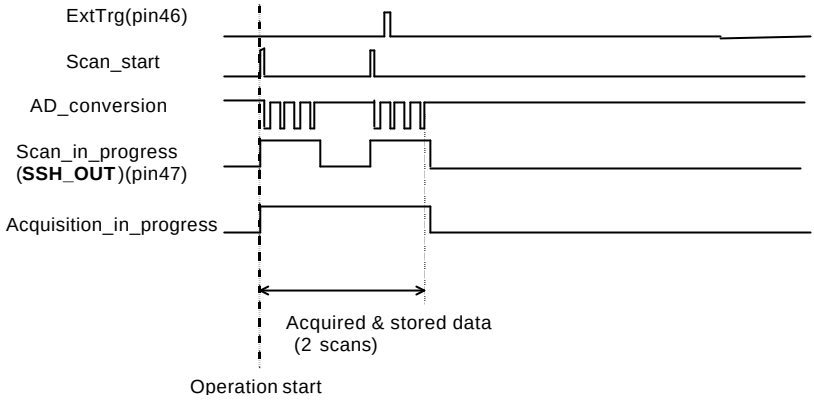


Figure 5.4 Pre-trigger with M_enable = 0 (trigger occurs before M scans)

(M_counter = M = 3, DIV_counter=4, SC_counter=0)

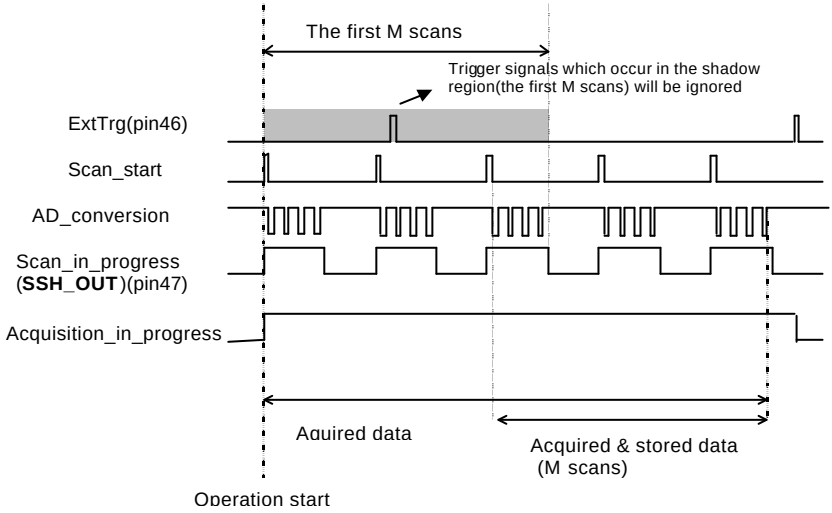


Figure 5.5 Pre-trigger with M_enable = 1

Note: The SC_counter must be set to 0 in pre-trigger acquisition mode.

Middle-Trigger Acquisition

Use middle-trigger acquisition in applications when you want to collect data before and after an external trigger event. The number of scans stored before the trigger is specified in M_counter, while the number of scans after the trigger is specified in SC_counter.

Like pre-trigger mode, the number of stored data could be fewer than the specified amount of data(DIV_counter *(M_counter+SC_counter)) if the external trigger occurs before M scans of data are converted. The **M_enable** bit in middle-trigger mode takes the same effect as in pre-trigger mode. If **M_enable** is set to 1, the tigger signal will be ignored until the first M scans of data are converted, and It assures user can get M+N scans of data under middle-trigger mode. However, if **M_enable** is set to 0, the trigger signal will be accepted in any time. Fig 5.6 shows the acquisition timing with M_enable=1.

(M_Counter=M=3, DIV_Counter=4, SC_Counter=N=1)

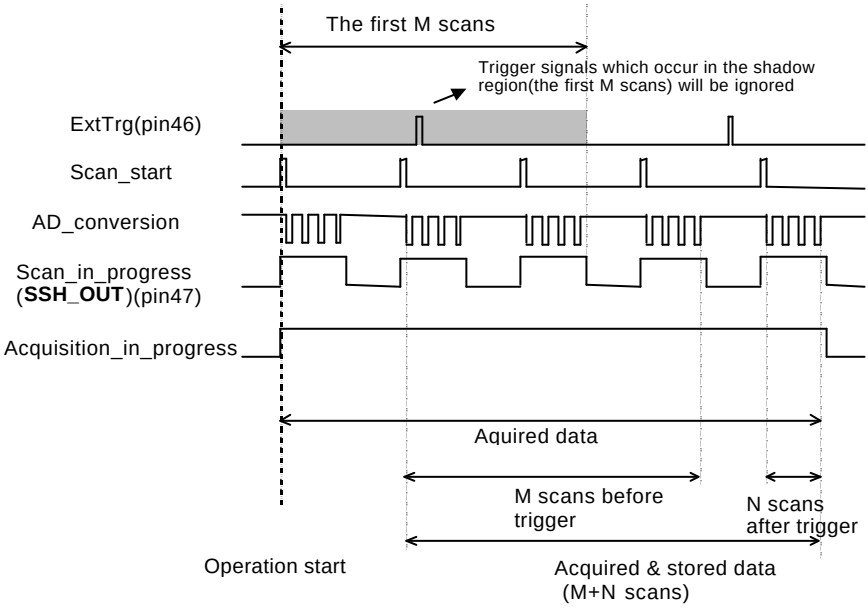


Figure 5.6 Middle trigger with M_enable = 1

If the external trigger event occurs when a scan is in progress, the stored N scans of data would include this scan. **And the first stored data will always be the first channel entry of a scan,** as illustrated in Fig5.7.

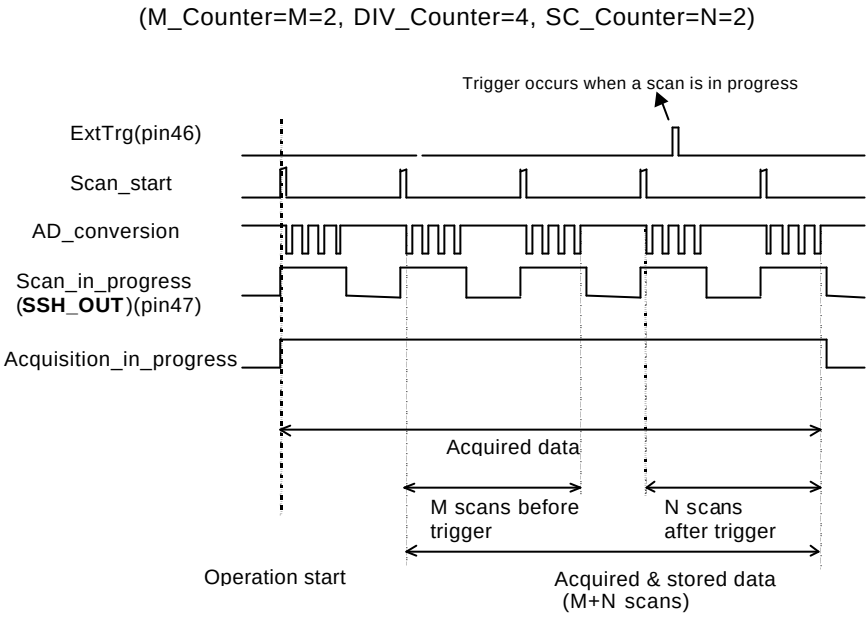


Figure 5.7 Middle trigger (trigger occurs when a scan is in progress)

Post-Trigger Acquisition

Use post-trigger acquisition in applications when you want to collect data after an external trigger event. The number of scans after the trigger is specified in SC_counter, as illustrated in fig 5.8. The total acquired data length = DIV_counter *SC_counter.

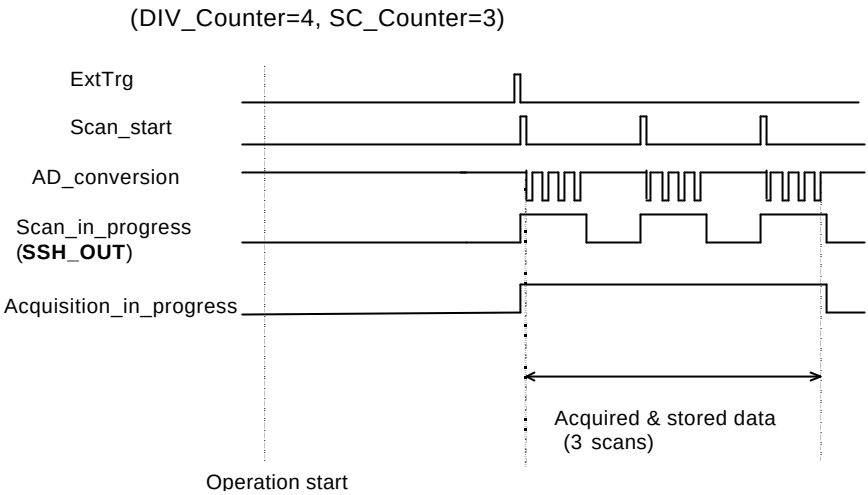


Figure 5.8 Post trigger

Delay Trigger Acquisition

Use delay trigger acquisition in applications when you want to delay the data collection after the occurrence of a specified trigger event. The delay time is controlled by the value which is pre-loaded in the **Delay_counter** (16bit)**.** Then the counter counts down on the rising edge of Delay_counter clock source after the trigger condition was met. The clock source can be software programmed either Timebase clock (24MHz) or A/D sampling clock (Timebase /SI2_counter). When the count reaches 0, the counter stops and cPCI-9116 starts to acquire data. The total acquired data length = DIV_counter * SC_counter.

(DIV_Counter=4, SC_Counter=3)

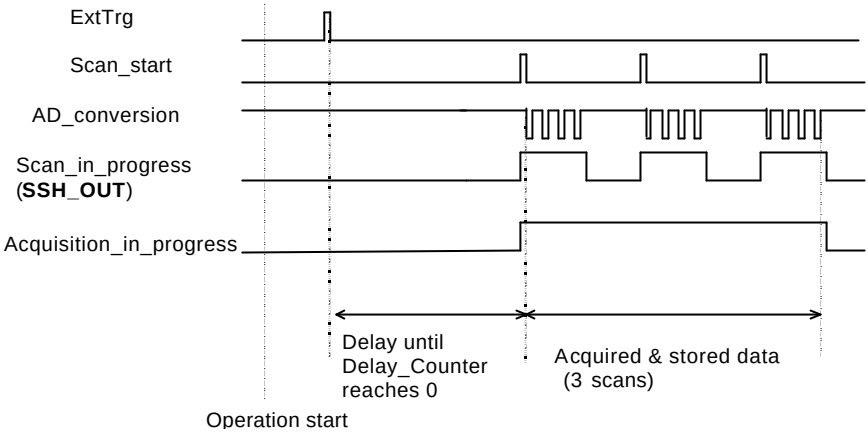


Figure 5.9 Delay trigger

Note: When the Delay_counter clock source is set to Timebase, the maximum delay time = 2^{16}/24M s = 2.73ms, and when the source is set to A/D sampling clock, the maximum delay time can be higher (2^{16} * SI2_counter / 24M).

Post-Trigger or Delay-trigger Acquisition with retrigger

Use post-trigger or delay-trigger acquisition with retrigger function in applications when you want to collect data after several external trigger events. The number of scans after each trigger is specified in SC_counter, and users could program **Retrig_no** to specify the retrigger numbers. Fig5.10 illustrates an example. In this example, 2 scans of data is acquired after the first trigger signal, then the board waits for the retrigger signal (retrigger signals which occur before the first 2 scans of data is acquired will be ignored). When the retrigger signal occurs, the board scans 2 scans of data more. The process repeats until specified amount of retrigger signals are detected. The total acquired data length = DIV_counter * SC_counter * Retrig_no.

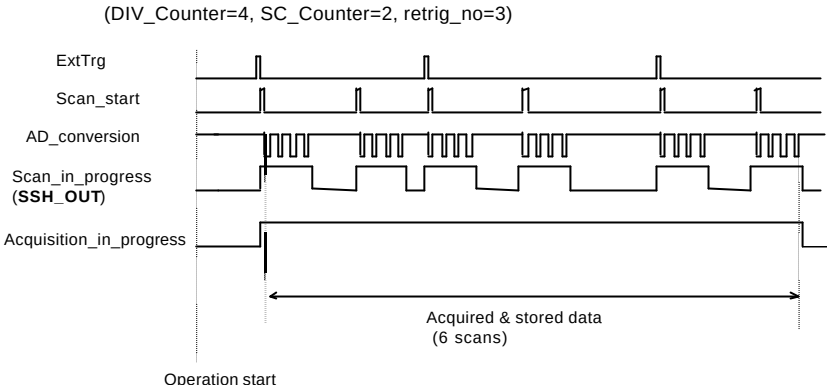


Figure 5.10 Post trigger with retrigger

5.1.4 A/D Data Transfer Modes

After the end of A/D conversion, A/D data are buffered in the **Data FIFO** memory. The FIFO size on cPCI-9116 is 1024 (1K) words. If the sampling rate is 10 KHz, the FIFO can buffer 102.4 ms analog signal. After the FIFO is full, the lasting coming data will be lost.

The data must be transferred to host memory after the data is ready and before the FIFO is full. In scan acquisition mode, there are 3 data transfer modes can be used. They will be described as follows.

EOC Interrupt Transfer

The cPCI-9116 provides traditional hardware end-of-conversion (EOC) interrupt capability. Under this mode, an interrupt signal is generated when the A/D conversion is ended and the data is ready to be read in the Data FIFO. The hardware interrupt will be asserted and its corresponding ISR (Interrupt Service Routine) will be invoked and executed. The ISR program can read the converted data. This method is suitable for data processing applications under real-time and fixed sampling rate.

FIFO Half-Full Interrupt Transfer

Sometimes, the applications do not need real-time processing, but the foreground program is too busy to poll the FIFO data. The FIFO half-full interrupt transfer mode is useful for the situation mentioned above.

Under this mode, an interrupt signal is generated when FIFO becomes half-full. It means there are 512 words data in the FIFO already. The ISR

can read a block of data when every interrupt occurring. This method is very convenient to read A/D in size of a “block” (512 words).

Note: In current version, EOC & FIFO half-full interrupt transfer modes don’t support pre-trigger and middle-trigger modes data acquisition. Users should use DMA transfer to work with pre-trigger or middle-trigger data acquisition.

DMA Transfer

PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum PCI bandwidth. The bus-mastering controller, which is built-in into the AMCC-5933 PCI controller, controls the PCI bus when it becomes the master of the bus. Bus mastering reduces the size of on-board memory and reduce the CPU loading because data is directly transferred to the computer’s memory without host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on PCI-bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard Data FIFO and then transfers the data to a user-defined DMA buffer memory in the computer. Please note that even when the acquired data length is less than the Data FIFO, the AD data will not be kept in the Data FIFO but directly transferred into host memory by bus-mastering DMA.

The DMA transfer mode is very complex to program. we recommend using a high level program library to manipulate this card. If you want to program the software which can handle the DMA bus master data transfer, please refer to more information about the PCI controller. (www. amcc. com)

Note: In DMA transfer mode, the maximum acquired data length in one acquisition could be up to 64M bytes(32 M samples), which is the limitation of the PCI controller. However, the memory that you allocate for data transfer must be continuous.

5.2 Digital Input and Output

To program digital I/O operation is fairly straight forward. The digital input operation is just to read data from the corresponding registers, and the digital output operation is to write data to the corresponding registers. The digital I/O registers' format are shown in section 4.9. The DO can be read back when reading the DI port. Note that the DIO data channel can only be read or written in form of 16 bits together. It is impossible to access individual bit channel.

5.3 General Purpose Timer/Counter Operation

An independent 16-bit up/down timer/counter is designed on FPGA for user's application. Fig 5.11 shows a simplified model of the timer/counter on cPCI-9116. It has the following features:

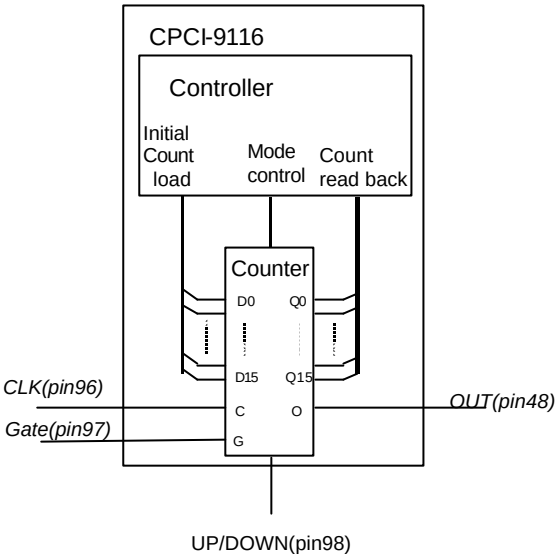


Figure 5.11 General-purpose Timer/Counter model (CLK, Gate, UP/DOWN can be software programmed external or internal)

- Count up/Count down controlled by hardware or software(low or 0: count down, high or 1: count up)
- Programmable counter CLK source selection(Internal 24MHz or External CLK input up to 20MHz)
- Programmable Gate selection(Internal or External. For Internal control, you can disable counting only by software. For External gate control, either software or setting Gate = low on pin97 of J1 disables the counting)
- Initial Count can be loaded from software
- Current count value can be read from software without affecting circuit operation

- Two programmable timer modes are provided and described as follows

Mode0: Interrupt on Terminal Count

Mode0 is typically used for event counting, as illustrated in fig 5.12. After the initial counts is written, OUT is initially low, and will remain low until the Counter counts to zero. OUT then goes high and will remain high until a new count is writen into the Counter .

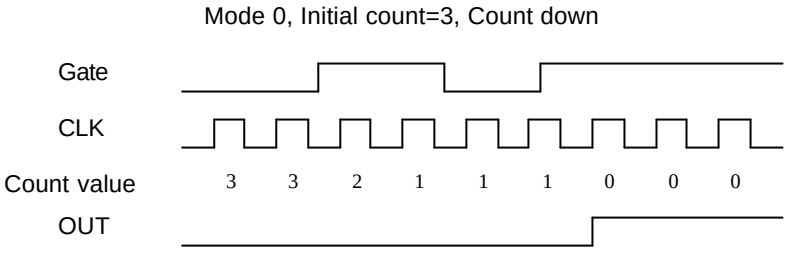


Figure 5.12 Mode 0 Operation

Mode1: Rate Generator

This mode functions like a divide-by-N counter, as illustrated in fig 5.13. After the initial counts is written, initially OUT is low. when the counter counts to 1, OUT goes high for one clock pulse. OUT then goes low again. The counter reloads the initial count and the process will be repeated.

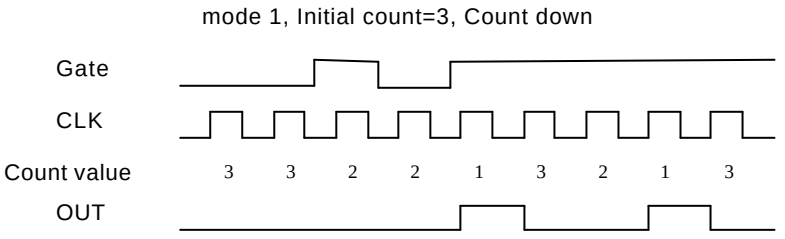


Figure 5.13 Mode 1 Operation

Note: In Mode 1 the initial count value N must be larger than one.

6

Software Utility & Calibration

This software CD provides a utility program, 9116util.exe which provides two functions: Calibration and Functional Testing. This utility is designed as menu-driven based windowing style. Not only the text messages are shown for operating guidance, but also has the graphic to indicate you how to set right hardware configuration. This utility is described in the following sections.

6.1 Running 9116util.exe

After finishing the DOS installation, you can execute the utility by typing as follows (assume your utility is located in \ADLINK\9116\DOS_BC\Util directory) :

C> cd \ADLINK\9116\DOS_BC\Util

C> 9116UTIL

the following diagram will be displayed on you screen. The message at the bottom of each window guides you how to select item, go to next step and change the default settings.

****** cPCI-9116 Utility Rev. 1.0 ******

<F1> : Calibration.

<F2> : Function testing.

<Esc>: Quit.

>>> Select function key F1 ~ F2, or press <Esc> to quit. <<<

6.2 Calibration

In data acquisition process, how to calibrate your measurement devices to maintain its accuracy is very important. Users can calibrate the analog input channels under the users' operating environment for optimizing the accuracy. This function will guide you to calibrate your cPCI-9116 to an accurate condition.

Note: For an environment with frequently large changes of temperature and vibration, a 3 months re-calibration interval is recommended. For laboratory conditions, 6 months to 1 year is acceptable.

6.2.1 What do you need

Before calibrating your cPCI-9116 card, you should prepare some equipment's for the calibration:

- A 5 1/2 digit multimeter (6 1/2 is recommended)
- A voltage calibrator or a very stable and noise free DC voltage generator

6.2.2 VR Assignment

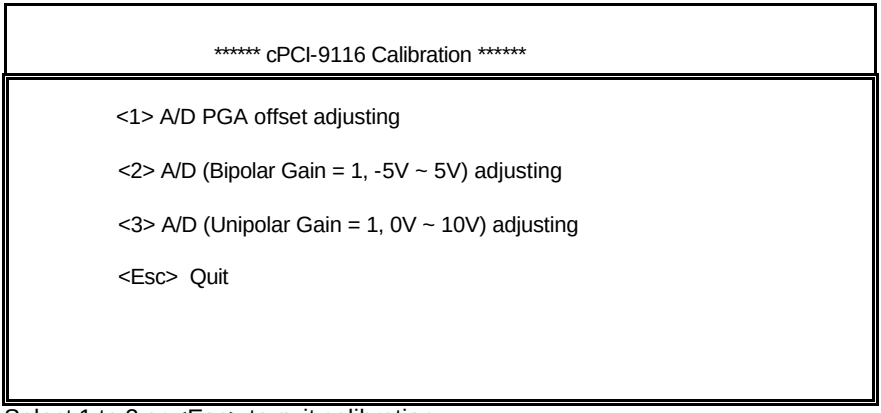
There are 4 variable resistors (VR) on the cPCI-9116 board to allow you making accurate adjustment on A/D channels. The function of each VR is specified as Table 6.1.

VR1	A/D unipolar offset adjustment
VR2	A/D bipolar offset adjustment
VR3	A/D full scale adjustment
VR4	PGA offset adjustment

Table 6.1 Function of VRs

6.2.3 A/D Adjustment

When you choose the calibration function from the main menu list, a calibration items menu is displayed on the screen. After you select one of the calibration items from the calibration items menu, a calibration window shows. The upper window shows the detailed procedures which have to be followed when you proceed the calibration. The instructions will guide you to calibrate each item step by step. The bottom window shows the layout of cPCI-9116. In addition, the proper Variable Resister (VR) will blink to indicate the related VR which needs to be adjusted for the current calibration step.



Select 1 to 3 or <Esc> to quit calibration.

6.2.3.1 PGA offset Calibration

1. Short the A/D channel 0(pin 2 of J1) to ground(pin51 of J1).
2. Use multi-meter to measure the voltage between **TP1** and **TP2** on board.
3. Adjust **VR4** to obtain the multi-meter value as close as possible to 0V.

6.2.3.2 Bipolar input Calibration

1. Calibrate the PGA offset as described in 6.2.3.1.
2. Connect A/D channel 0 (pin 2 of J1) to ground (pin 51 of J1), and Applied a precise +5V to A/D channel 1 (pin 3 of J1).

3. Trim **VR2** to obtain the reading of A/D channel 0 flicks between 0 to 1, and Trim **VR3** to obtain reading of A/D channel 1 flicks between 32766~32767.

6.2.3.3 Unipolar input Calibration

1. Calibrate the PGA offset as described in 6.2.3.1.

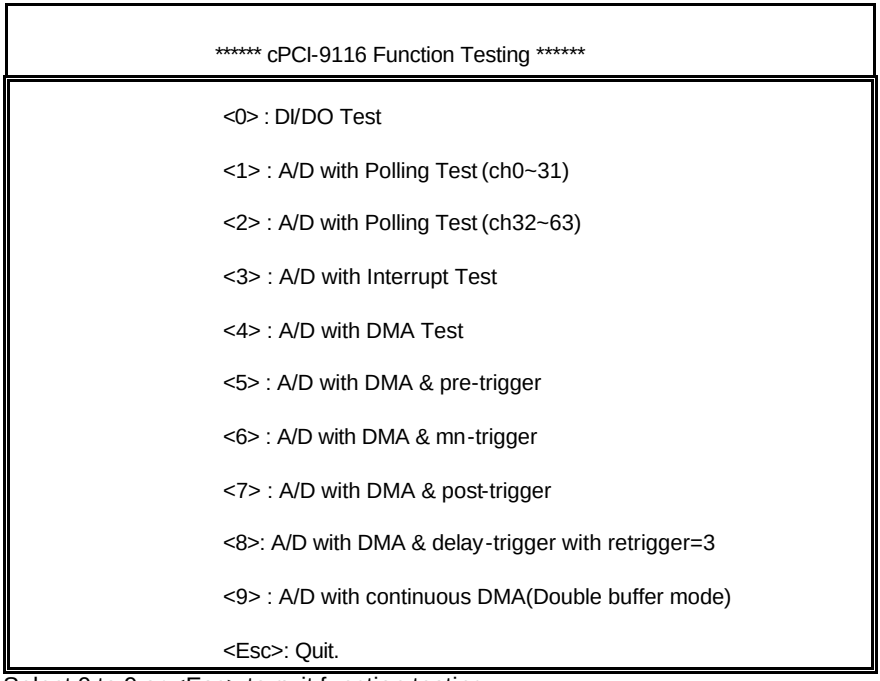
2. Applied a precise +5 V input signal to A/D channel 1 (pin 3 of J1).

3. Trim ***VR1*** to obtain reading flicking between 0~1.

6.3 Functional Testing

This function is used to test the functions of cPCI-9116, it includes Digital I/O testing, A/D polling test, A/D Interrupt Test, A/D with DMA test, A/D with DMA & pre-trigger test, A/D with DMA & mn-trigger test, A/D with DMA & post-trigger test, A/D with DMA & delay-trigger with retrigger=3 test, and A/D with continuous DMA test(Double buffer mode).

When you choose one of the testing function from the functions menu, a diagram is displayed on the screen. The figure below is the function testing menu window.



Select 0 to 9 or <Esc> to quit function testing

A calibration utility is supported in the software CD which is included in the product package. The detailed calibration procedures and description can be found in the utility. Users only need to run the software calibration utility and follow the procedures. You will get the accurate measure data.

In normal condition, the cPCI-9116 already calibrated by factor before it is shipped out. So users do not need to calibrate your cPCI-9116 when you get it.

Product Warranty/Service

ADLINK warrants that equipment furnished will be free from defects in material and workmanship for a period of one year from the date of shipment. During the warranty period, we shall, at our option, either repair or replace any product that proves to be defective under normal operation.

This warranty shall not apply to equipment that has been previously repaired or altered outside our plant in any way as to, in the judgment of the manufacturer, affect its reliability. Nor will it apply if the equipment has been used in a manner exceeding its specifications or if the serial number has been removed.

ADLINK does not assume any liability for consequential damages as a result from our product uses, and in any event our liability shall not exceed the original selling price of the equipment. The remedies provided herein are the customer's sole and exclusive remedies. In no event shall ADLINK be liable for direct, indirect, special or consequential damages whether based on contract of any other legal theory.

The equipment must be returned postage-prepaid. Package it securely and insure it. You will be charged for parts and labor if the warranty period is expired or the product is proves to be misuse, abuse or unauthorized repair or modification.