A-8112DG/HG

Enhanced Multi-Function Card
Hardware Manual

Warranty

All products manufactured by ICP DAS are warranted against defective materials for a period of one year from the date of delivery to the original purchaser.

Warning

ICP DAS assume no liability for damages consequent to the use of this product. ICP DAS reserves the right to change this manual at any time without notice. The information furnished by ICP DAS is believed to be accurate and reliable. However, no responsibility is assumed by ICP DAS for its use, nor for any infringements of patents or other rights of third parties resulting from its use.

Copyright

Tables of Contents

1. Introduction 4

1.1 General Description 4

1.2 Features 4

1.3 Specifications 5

1.3.1 Power Consumption 5

1.3.2 Analog Inputs 5

1.3.3 A/D Converter 5

1.3.4 DA Converter 6

1.3.5 Digital I/O 6

1.3.6 Interrupt Channel 6

1.3.7 Programmable Timer/Counter 7

1.3.8 Direct Memory Access Channel (DMA) 7

1.4 Applications 8

1.5 Product Check List 8

1.6 Software Installation 9

2. Hardware Configuration 10

2.1 Board Layout 10

2.2 I/O Base Address Setting 11

2.3 Jumper Setting 12

2.3.1 JP1 : D/A Internal Reference Voltage Selection 12

2.3.2 JP2 : D/A Int/Ext Ref Voltage Selection 13

2.3.3 JP3 : Single-ended 13

2.3.4 JP4 : A/D Trigger Source Selection 14

2.3.5 JP5 : Interrupt Level Selection 14

2.3.6 JP6 : User Timer/Counter Clock Input Selection 15

2.3.7 JP7 : DMA DACK Selection, JP8 : DMA DRQ Selection 16

2.4 I/O Register Address 17

2.4.1 8254 Counter 18

2.4.2 A/D Input Buffer Register 18

2.4.3 D/A Output Latch Register 19

2.4.4 D/I Input Buffer Register 20

2.4.5 Clear Interrupt Request 20

2.4.6 A/D Gain Control Register 21

2.4.7 A/D Multiplex Control Register 22
2.4.8 A/D Mode Control Register 23
2.4.9 A/D Software Trigger Control Register 24
2.4.10 D/O Output Latch Register 25
2.5 Digital I/O 26
2.6 8254 Timer/Counter 27
2.7 A/D Conversion 28
2.7.1 A/D conversion flow 29
2.7.2 A/D Conversion Trigger Modes 30
2.7.3 A/D Transfer Modes 30
2.7.4 Using software trigger and polling transfer 31
2.8 D/A Conversion 32
2.9 Analog Input Signal Connection 33
2.10 Using DB-8225 CJC Output 34
3. Connector 35
3.1 CN1/CN2/CN3 Pin Assignment 35
3.2 Daughter Board 37
3.2.1 DB-8225 37
3.2.2 DB-37 37
3.2.3 DB-16P 37
3.2.4 DB-16R 37
4. Calibration VR Description 38

1. Introduction

1.1 General Description

The A-8112DG/HG is a high performance, multifunction analog, digital I/O board for the PC AT compatible computer. The A-8112DG provides low gain (0.5, 1, 2, 4, 8). The A-8112HG provides high gain (0.5, 1, 5, 10, 50, 100, 500, 1000). The A-8112DG/HG contains a 12-bit ADC with up to 16 single-ended analog inputs. The maximum sample rate of A/D converter is about 100Ksample/sec. There are two 12-bits DAC with voltage outputs, 16 channels of TTL-compatible digital input, 16 channels of TTL-compatible digital output and one 16-bit counter/timer channel for timing input and output.

Using ASC-TI486/33M CPU board of ICP as a target PC based system, the performance of A/D conversion is given as below:

- **Polling mode : about 100Ksample/sec (with single-task OS)**
- **Interrupt mode : about 60Ksample/sec (with single-task OS)**
- **DMA mode : about 100Ksample/sec (with single-task OS)**

1.2 Features

- The maximum sample rate of A/D converter is about 100 K sample/sec
- Software selectable input ranges
- PC AT compatible ISA bus
- A/D trigger mode : software trigger , pacer trigger, external trigger
- 16 single-ended analog input channels
- Programmable high gain : 0.5,1,5,10,50,100,500,1000 (A-8112HG)
- Programmable low gain : 0.5,1,2,4,8 (A-8112DG)
- 2 channels 12-bit D/A voltage output
- 16 digital input /16 digital output (TTL compatible)
- Interrupt handling
- Bipolar/unipolar operation
- 1 channel general purpose programmable 16 bits timer/counter

1.3 Specifications

1.3.1 Power Consumption :

- +5V @960 mA maximum, A-8112DG/HG
- Operating temperature : -20°C ~ 60°C

1.3.2 Analog Inputs

- Channels : 16 single-ended
- Input range : (software programmable)

A-8112DG:bipolar : ±10V,±5V, ±2.5V, ±1.25V, ±0.0625V

unipolar : 0~10V, 0~5V, 0~0.2.5V, 0~1.25.V

A-8112HG:bipolar : ±10,±5V,±1V, ±0.5V, ±0.1V, ±0.05V, ±0.01V, ± 0.005V

unipolar : 0-~10V, 0~1V, 0~0.1V, 0~0.01V

- Input current : 250 nA max (125 nA typical) at 25 deg.
- On chip sample and hold
- Over voltage : continuous single channel to **70Vp-p**
- Input impedance : 10^{10} Ω // 6pF

Caution : refer to Sec. 2.9 first

1.3.3 A/D Converter

- Type : successive approximation , Burr Brown ADS 774 or SIPEX-SP774B (equivalent)
- Conversion time : 8 microsec.
- Accuracy : +/- 1 bit
- Resolution : 12 bits

1.3.4 DA Converter

- Channels : 2 independent
- Type : 12 bit multiplying , Analog device AD-7541
- Linearity : +/- 1/2 bit
- Output range : 0~5V or 0~10V jumper selected , may be used with other AC or DC reference input Maximum output limit +/- 10V
- Output drive : +/- 5mA
- Settling time : 0.6 microseconds to 0.01% for full scale step

1.3.5 Digital I/O

- Output port : 16 bits, TTL compatible
- Input port : 16 bits, TTL compatible

1.3.6 Interrupt Channel

- Level : 3,4,5,6,7,9,10,11,12,14,15, jumper selectable
- Enable : Via control register

1.3.7 Programmable Timer/Counter

- Type : 82C54 -8 programmable timer/counter
- Counters : The counter1 and counter2 are cascaded as a 32 bits pacer timer The counter0 is used as user timer/counter. The software driver use counter0 to implement a machine independent timer.
- Clock input frequency : DC to 10 MHz
- Pacer output : 0.00047Hz to 0.5MHz
- Input ,gate : TTL compatible
- Internal Clock : 2M Hz

1.3.8 Direct Memory Access Channel (DMA)

- Level : CH1 or CH3, jumper selectable
- Enable : via DMA bit of control register
- Termination : by interrupt on T/C
- Transfer rate : 100K conversions/sec.

1.4 Applications

- Signal analysis
- FFT & frequency analysis
- Transient analysis
- Production test
- Process control
- Vibration analysis
- Energy management
- Industrial and lab. measurement and control

1.5 Product Check List

The package includes the following items:

- A-8112DG/HG multifunction card
- A-8112DG/HG utility diskette

Attention !

If any of these items is missing or damaged, contact the dealer who provides you this product. Save the shipping materials and carton in case you want to ship or store the product in the future.

1.6 Software Installation

The A-8112DG/HG hardware is supported by the A-822PGL/PGH software. The driver defines "**A822_Mode"= 0** and"**A8112_Mode"= 1**; and provides a function

Word A822_SetCardModel (WORD wCardMode)

to set the driver using corresponding configuration.

When using the A-822 software to drive A-8112DG/HG, please refer to the A-8112 demo programs and call **A822_SetCardModel (A8112_Mode)** to set the driver in correct mode.

Insert the enclosed CD

For Windows Users

The installation menu should open automatically. If not, double-click "Auto32.exe" in CD:\NAPDOS\ to start the installation menu, select

"Install Toolkits (Software) / Manuals" >> **"ISA Bus DAQ Card"** >> **"A-822PGH/PGL, A8112DG/HG"**>> **"DLL and OCX for Windows XX"**.

"XX" means the user's OS. Run the executable file in the driver folder in pop-up window.

You can also install the driver from CD: \NAPDOS\ISA\A822\DLL_OCX\ and find A-8112 demo programs in the same directory.

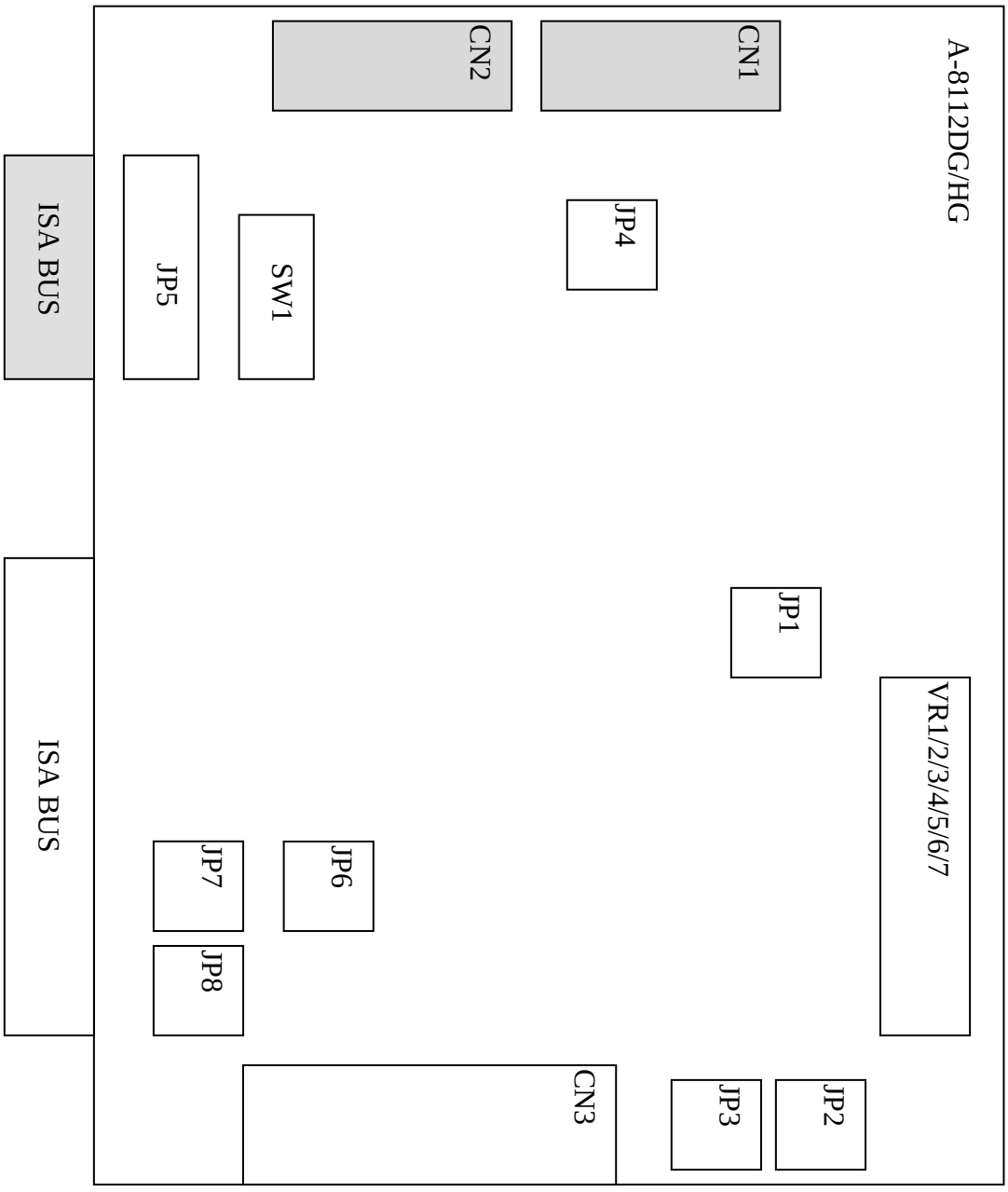
There are more reference documentations in CD: \NAPDOS\ISA\Manual\ for Plug and Play steps in Win2000/XP or resource conflict checking.

For DOS Users

Please refer to the A-8112 demo programs in NAPDOS\ISA\A822\DOS\A822\DEMO\.

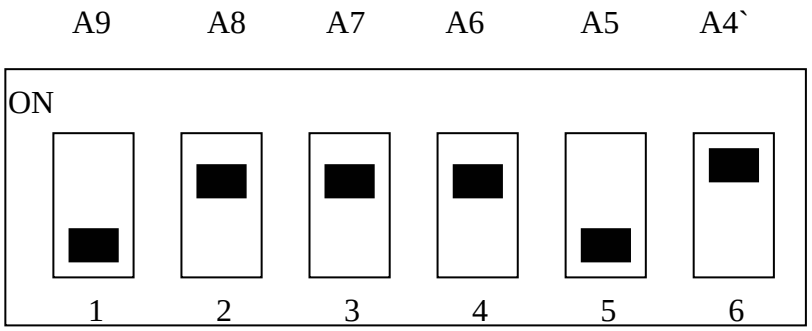
2. Hardware Configuration

2.1 Board Layout



2.2 I/O Base Address Setting

The A-8112DG/HG occupies 16 consecutive locations in I/O address space.
The base address is set by DIP switch SW1. The default address is 0x220.



SW1 : BASE ADDRESS

BASE ADDR	A9	A8	A7	A6	A5	A4
200-20F	OFF	ON	ON	ON	ON	ON
210-21F	OFF	ON	ON	ON	ON	OFF
220-22F(☑)	OFF	ON	ON	ON	OFF	ON
230-23F	OFF	ON	ON	ON	OFF	OFF
:	:	:	:	:	:	:
300-30F	OFF	OFF	ON	ON	ON	ON
:	:	:	:	:	:	:
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

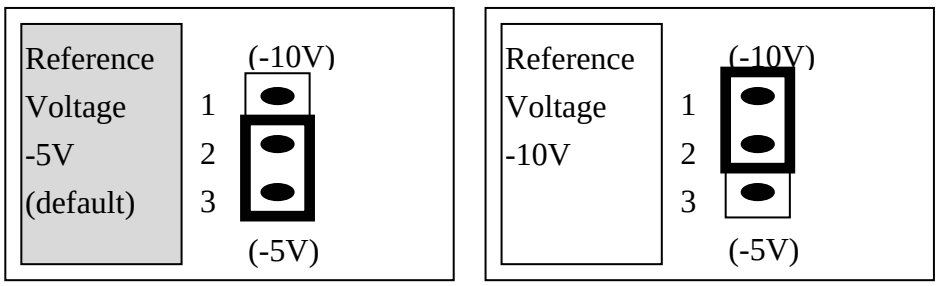
(☑) : default base address is 0x220

The PC I/O port mapping is given below.

ADDRESS	Device	ADDRESS	DEVICE
000-1FF	PC reserved	320-32F	XT Hard Disk
200-20F	Game/control	378-37F	Parallel Printer
210-21F	XT Expansion Unit	380-38F	SDLC
238-23F	Bus Mouse/Alt. Bus Mouse	3A0-3AF	SDLC
278-27F	Parallel Printer	3B0-3BF	MDA/Parallel Printer
2B0-2DF	EGA	3C0-3CF	EGA
2E0-2E7	AT GPIB	3D0-3DF	CGA
2E8-2EF	Serial Port	3E8-3EF	Serial Port
2F8-2FF	Serial Port	3F0-3F7	Floppy Disk
300-31F	Prototype Card	3F8-3FF	Serial Port

2.3 Jumper Setting

2.3.1 JP1 : D/A Internal Reference Voltage Selection

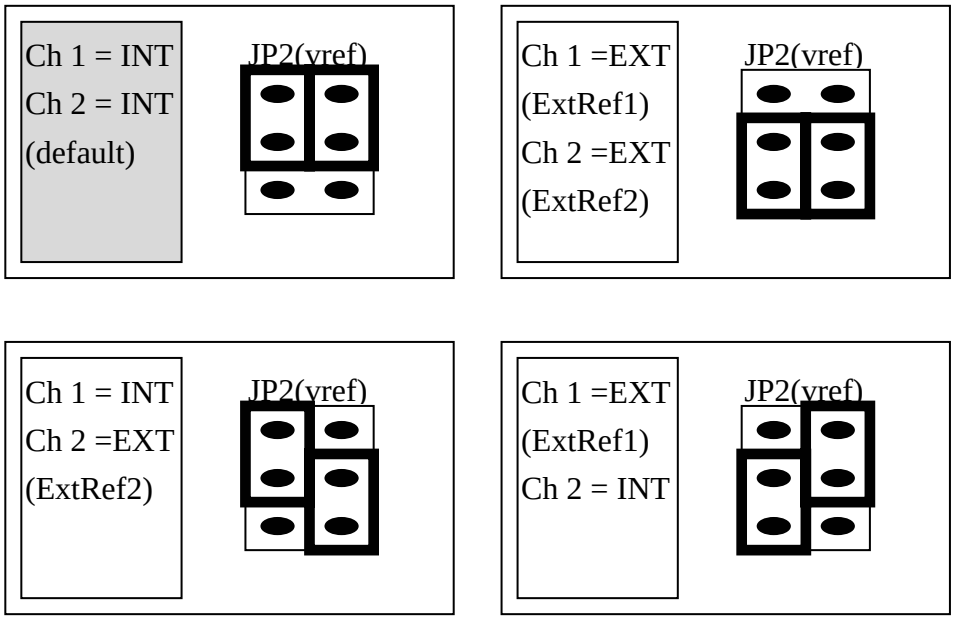


Select (-5V) : D/A voltage output = 0 to 5V (both channels)

Select (-10V) : D/A voltage output = 0 to 10V (both channels)

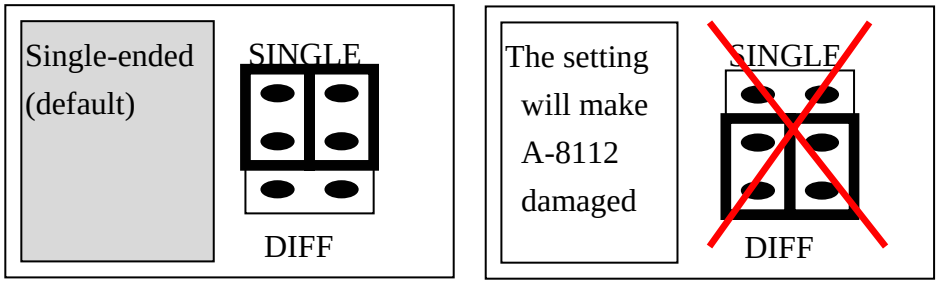
JP1 is validate only if JP2 select D/A internal reference voltage

2.3.2 JP2 : D/A Int/Ext Ref Voltage Selection



If JP2 select **internal reference**, then JP1 select **-5V/-10V** internal reference voltage.
If JP2 select **external reference**, then **ExtRef1, CN3 pin 31**, is the external reference voltage for DA channel 1; and **ExtRef2, CN3 pin 12**, is the external reference voltage for DA Channel 2. If user provides AC +/- 10V external reference voltage, the D/A output voltage may be AC -/+ 10V

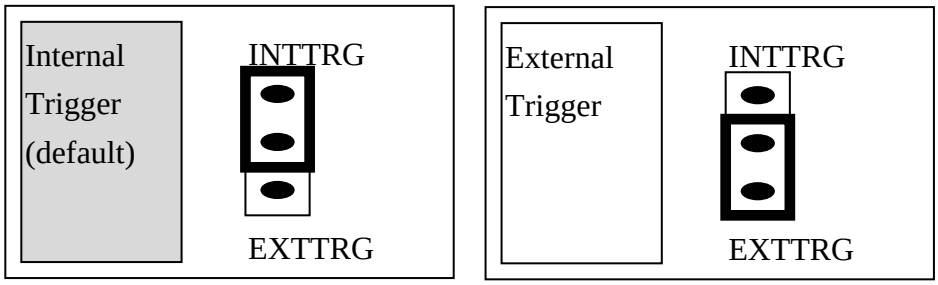
2.3.3 JP3 : Single-ended



The A-8112DG/HG offers 16 single-ended analog input channels. The JP3 only can be selected at single-ended.

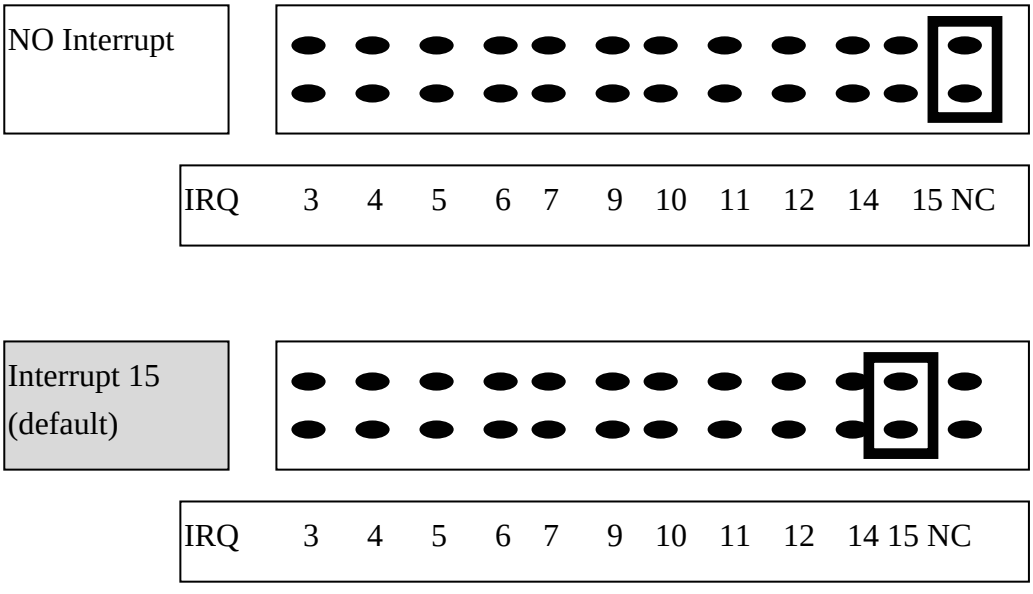
Setting JP3 at DIFF position will make A-8112 damaged forever.

2.3.4 JP4 : A/D Trigger Source Selection



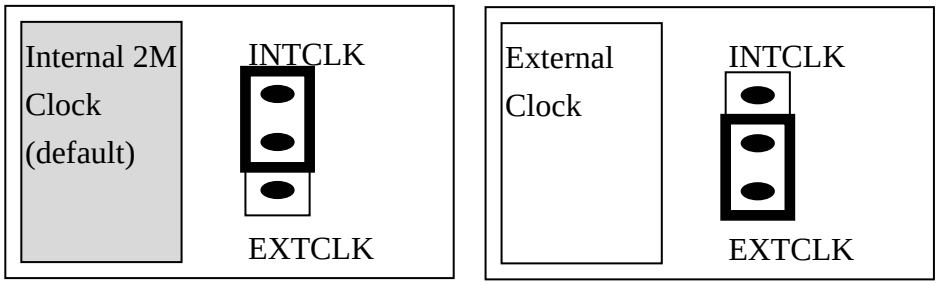
The A-8112DG/HG supports two trigger type, **internal trigger** and **external trigger.** The external trigger comes from **ExtTrg, CN3 pin 17**. There are two types of internal trigger, **software trigger** and **pacer trigge**r. The details information is given in section 2.4.8.

2.3.5 JP5 : Interrupt Level Selection



The interrupt channel **<u>can not be shared.</u>** The A-822 software driver can support 8 boards in one system but only **2 of these cards** can use interrupt transfer function.

2.3.6 JP6 : User Timer/Counter Clock Input Selection



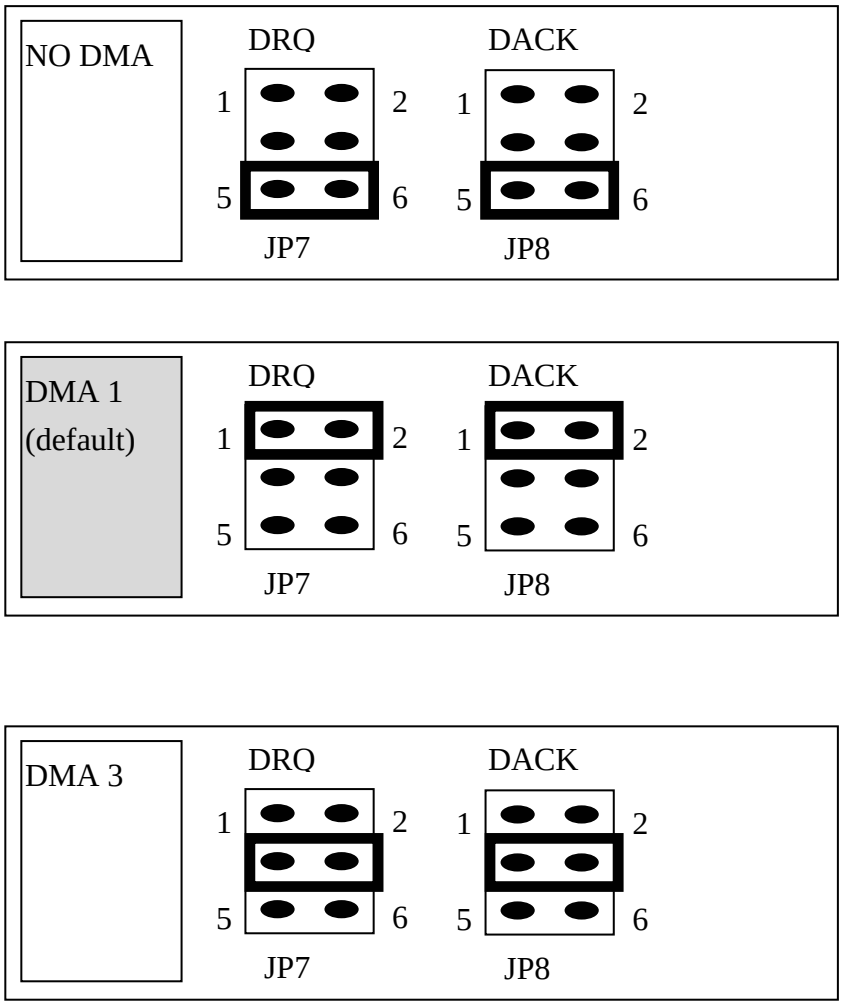
The A-8112DG/HG has 3 independent 16 bits timer/counter. The cascaded counter1 and counter2 are used as **a pacer timer**. The counter0 can be used as a user programmable timer/counter. The user programmable timer/counter can select **2M internal clock** or **external clock ExtCLK, CN3 pin 37**. The block diagram is given in section 2.6. The clock source must be very **stable.** It is recommended to use internal 2M clock.

The A-822 software driver uses the counter0 as a machine independent timer. If user's program calls **A822_Delay()** subroutine, the counter0 will be programmed as a machine independent timer. The detail information is given in section 2.6.

NOTE : if using A822_Delay(), the JP6 must select internal 2M clock.

2.3.7 JP7 : DMA DACK Selection,

JP8 : DMA DRQ Selection



The DMA channel can not shared. The A-822 software driver can support 8 boards in one PC based system, but only **two of these boards** can use DMA transfer function.

2.4 I/O Register Address

The A-8112DG/DG occupies 16 consecutive PC I/O addresses. The following table lists the registers and their locations.

Address	Read	Write
Base+0	8254 Counter 0	8254 Counter 0
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control
Base+4	A/D Low Byte	D/A Channel 0 Low Byte
Base+5	A/D High Byte	D/A Channel 0 High Byte
Base+6	DI Low Byte	D/A Channel 1 Low Byte
Base+7	DI High Byte	D/A Channel 1 High Byte
Base+8	Reserved	A/D Clear Interrupt Request
Base+9	Reserved	A/D Gain Control
Base+A	Reserved	A/D Multiplexer Control
Base+B	Reserved	A/D Mode Control
Base+C	Reserved	A/D Software Trigger Control
Base+D	Reserved	DO Low Byte
Base+E	Reserved	DO High Byte
Base+F	Reserved	Reserved

2.4.1 8254 Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about 8254, please refer to Intel‘s “Microsystem Components Handbook”.

Address	**Read**	**Write**
Base+0	8254 Counter 0	8254 Counter 0
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control

2.4.2 A/D Input Buffer Register

(READ) Base+4 : A/D Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+5 : A/D High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	BUSY	D11	D10	D9	D8

A/D 12 bits data : D11…..D0, D11=MSB, D0=LSB

BUSY =1 : A/D 12 bits data is busy

=0 : A/D 12 bits data is ready

The low 8 bits A/D data are stored in address BASE+4 and the high 4 bits data are stored in address BASE+5. The BUSY bit is used as a indicator for A/D conversion. **When a A/D conversion is completed, the BUSY bit will be clear to zero.**

2.4.3 D/A Output Latch Register

(WRITE) Base+4 : Channel 0 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+5 : Channel 0 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

(WRITE) Base+6 : Channel 1 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+7 : Channel 1 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

D/A 12 bits output data : D11..D0, D11=MSB, D0=LSB, X=don‘t care

The D/A converter will convert the 12 bits digital data to analog output. The low 8 bits of **D/A channel 0** are stored in address BASE+4 and high 4 bits are stored in address BASE+5. The address BASE+6 and BASE+7 store the 12 bits data for **D/A channel 1**. The D/A output latch registers are designed as a **“double buffered”** structure, so the analog output latch registers will be updated until the high 4 bits digital data are written. If the user sends the high 4 bits data first, the DA 12 bits output latch registers will update at once. So the low 8 bits will be the previous data latched in register. **This action will cause an error on DA output voltage**. **So the user must send low 8 bits first and then send high 4 bits to update the 12 bits AD output** latch register.

NOTE : Send low 8 bits first, then send high 4 bits.

2.4.4 D/I Input Buffer Register

(READ) Base+6 : D/I Input Buffer Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+7 : D/I Input Buffer High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

D/I 16 bits input data : D15..D0, D15=MSB, D0=LSB

The A-8112DG/HG provides 16 TTL compatible digital inputs. The low 8 bits are stored in address BASE+6. The high 8 bits are stored in address BASE+7.

2.4.5 Clear Interrupt Request

(WRITE) Base+8 : Clear Interrupt Request Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don‘t care, XXXXXXXX=any 8 bits data is validate

If A-8112DG/HG is working in the interrupt transfer mode, an on-board hardware status bit will be set after each A/D conversion. This bit must be **clear by software** before next hardware interrupt. Writing any value to address BASE+8 will clear this hardware bit and the hardware will generate another interrupt when next A/D conversion is completed.

2.4.6 A/D Gain Control Register

(WRITE) Base+9 : A/D Gain Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	GAIN3	GAIN2	GAIN1	GAIN0

The Only difference between A-8112DG and A-8112HG is the **GAIN** control function. The **A-8112DG provides gain factor of 1/2/4/8** and **A-8112HG provides 1/10/100/1000.** The gain control register control the gain of A/D input signal. Bipolar/Unipolar will affect the gain factor. It is important to select the correct gain-control-code according to Bipolar/Unipolar input.

NOTE : If gain control code changed, the hardware need to delay extra gain settling time. The gain settling time is different for different gain control code. **The DOS driver does not take care of the gain settling time, so the user needs to delay the gain settling time if gain changed.** If the application program needs to run in different machines, the user needs to implement a machine independent timer. The software driver, **A822_delay(),** is designed for this purpose. If user uses this subroutine then the counter0 introduced in sec 2.6 is reserved by software driver to implement this machine independent timer.

A-8112DG GAIN CONTROL CODE TABLE

BI/UNI	Settling Time	GAIN	Input Range	GAIN3	GAIN2	GAIN1	GAIN0
BI	23 us	1	+/- 5V	0	0	0	0
BI	23 us	2	+/- 2.5V	0	0	0	1
BI	25 us	4	+/- 1.25V	0	0	1	0
BI	28 us	8	+/- 0.0625V	0	0	1	1
UNI	23 us	1	0V ~ 10V	0	1	0	0
UNI	23 us	2	0V ~ 5V	0	1	0	1
UNI	25 us	4	0V ~ 2.5V	0	1	1	0
UNI	28 us	8	0V ~ 1.25V	0	1	1	1
BI	23 us	0.5	+/- 10V	1	0	0	0

BI=Bipolar, UNI=Unipolar, X=don‘t care, N/A=not available

A-8112HG GAIN CONTROL CODE TABLE

BI/UN	Settling Time	GAIN	Input Range	GAIN3	GAIN2	GAIN1	GAIN0
BI	23 us	1	+/- 5V	0	0	0	0
BI	28 us	10	+/- 0.5V	0	0	0	1
BI	140 us	100	+/- 0.05V	0	0	1	0
BI	1300 us	1000	+/- 0.005V	0	0	1	1
UNI	23 us	1	0 ~ 10V	0	1	0	0
UNI	28 us	10	0 ~ 1V	0	1	0	1
UNI	140 us	100	0 ~ 0.1V	0	1	1	0
UNI	1300 us	1000	0 ~ 0.01V	0	1	1	1
BI	23 us	0.5	+/- 10V	1	0	0	0
BI	28 us	5	+/- 1V	1	0	0	1
BI	140 us	50	+/- 0.1V	1	0	1	0
BI	1300 us	500	+/- 0.01V	1	0	1	1

BI=Bipolar, UNI=Unipolar, X=don‘t care, N/A=not available

2.4.7 A/D Multiplex Control Register

(WRITE) Base+A : A/D Multilexer Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	Ch8 ~15	Ch 0 ~7	X	D2	D1	D0

A/D input channel selection: X=don‘t care; D2 … D0 are used to select active channel

Bit5: Bit4 = 0: 1 : the target channel is in channel 0 ~ 7

Bit5: Bit4 = 1: 0 : the target channel is in channel 8 ~15

Caution: setting Bit5 and Bit4 to 1 simultaneously will make A-8112 damaged forever.

When Bit5: Bit4 = 0: 1, D2 … D0 = the selected channel number

When Bit5: Bit4 = 1: 0, (D2 … D0 + 8) = the selected channel number.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	The selected channel number
0	0	0	1	0	0	0	0	Channel 0
0	0	1	0	0	0	0	0	Channel 8
0	0	0	1	0	1	0	1	Channel 5
0	0	1	0	0	1	0	1	Channel 13

NOTE: The settling time of multiplexer depend on source resistance of input sources.

source resistance = about 0.1K ohm → settling time = about 3 us.

source resistance = about 1K ohm → settling time = about 5 us.

source resistance = about 10K ohm → settling time = about 10 us.

source resistance = about 100K ohm → settling time = about 100 us.

Sec 2.4.6 gives information about how to delay the settling time.

2.4.8 A/D Mode Control Register

(WRITE) Base+B : A/D Mode Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	D2	D1	D0

X=don‘t care

JP4 Select Internal Trigger							
Mode Select			Trigger Type		Transfer Type		
D2	D1	D0	Software Trig	Pacer Trig	Software	Interrupt	DMA
0	0	0	X	X	X	X	X
0	0	1	Select	X	Select	X	X
0	1	0	X	Select	X	X	Select
1	1	0	X	Select	Select	Select	X

X=disable

JP4 Select External Trigger						
Mode Select			Trigger Type	Transfer Type		
D2	D1	D0	External Trigger	Software	Interrupt	DMA
0	0	0	X	X	X	X
0	0	1	X	X	X	X
0	1	0	Select	X	X	Select
1	1	0	Select	Select	Select	X

The A/D conversion operation can be divided into 2 stage, **trigger stage and transfer stage**. The trigger stage will generate a trigger signal to A/D converter and the transfer stage will transfer the result to the CPU.

The trigger method may be **internal trigger** or **external trigger.** The internal trigger can be **software trigger** or **pacer trigger. The software trigger is very simple but can not control the sampling rate very precisely.** In software trigger mode, the program issues a software trigger command (sec 2.4.9) any time needed. Then the program will poll the A/D status bit until the ready bit is 0(sec 2.4.2).

The pacer trigger can control the sampling rate very precisely. So the converted data can be used to reconstruct the waveform of analog input signal. In pacer trigger mode, the pacer timer (sec 2.6) will generate trigger signals to A/D converter periodic. These converted data can be transfer to the CPU by polling or interrupt or DMA transfer method.

The software driver provides three data transfer methods, **polling, interrupt and DMA.** The polling subroutine, A822_AD_PollingVar() or A822_AD_PollingArray(), set A/D mode control register to **0x01.** This control word means software trigger and polling transfer. The interrupt subroutine, A822_AD_INT_START(…), set A/D mode control mode register to **ox06.** This control word means pacer trigger and interrupt transfer. The DMA subroutine, A822_AD_DMA_START(…), set A/D mode control register to **0x02**. This control word means pacer trigger and DMA transfer.

Please refer to sec. 2.7 for detail information.

2.4.9 A/D Software Trigger Control Register

(WRITE) Base+C : A/D Software Trigger Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don‘t care, XXXXXXXX=any 8 bits data is validate

The A/D converter can be triggered by software trigger or pacer trigger. The details information is given in sec. 2.4.8 and sec. 2.7. Writing any value to address BASE+C will generate a trigger pulse to A/D converter and initiated an A/D conversion operation. The address BASE+5 offers a busy bit to indicate an A/D conversion complete.

The software driver uses this control word to detect the A-8112DG/HG hardware board. **The software initiates a software trigger and checks the busy bit**. If the busy bit can not clear to zero in a fixed time, the software driver will return an error message. If the I/O BASE address setting error, the busy bit will not be clear to zero. The software driver, **A822_CheckAddress()**, use this method to detect the correctness of I/O BASE address setting

2.4.10 D/O Output Latch Register

(WRITE) Base+D : D/O Output Latch Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+E : D/O Output Latch High Byte Data Format

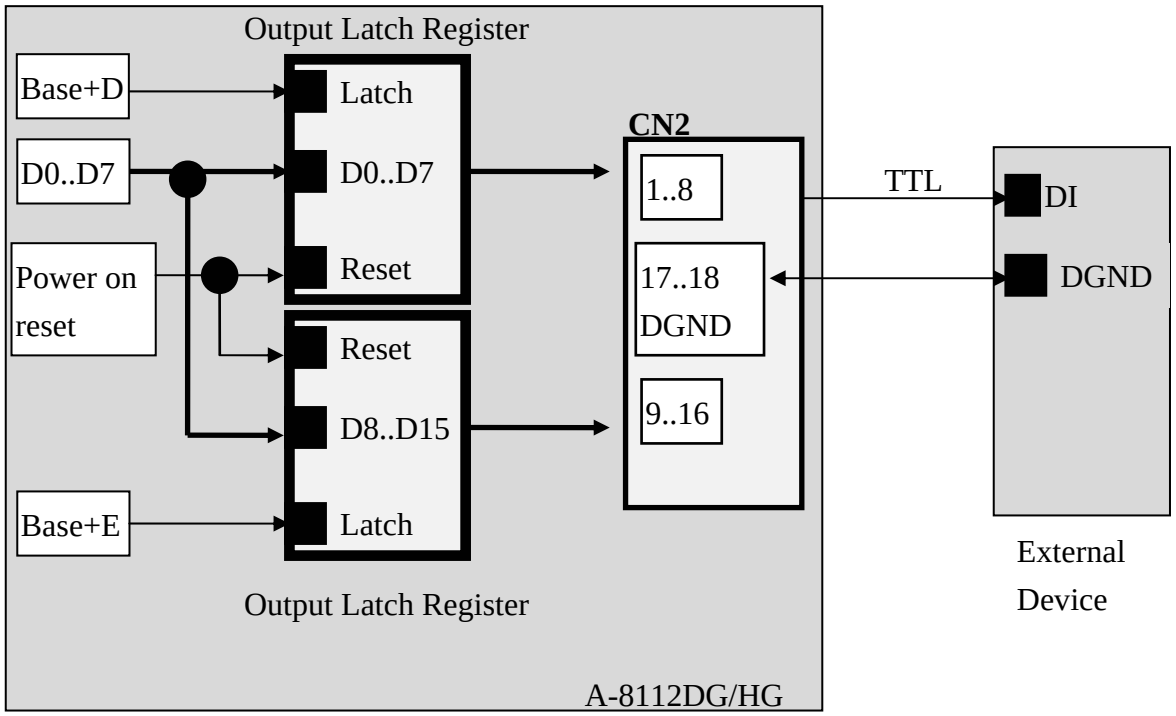
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

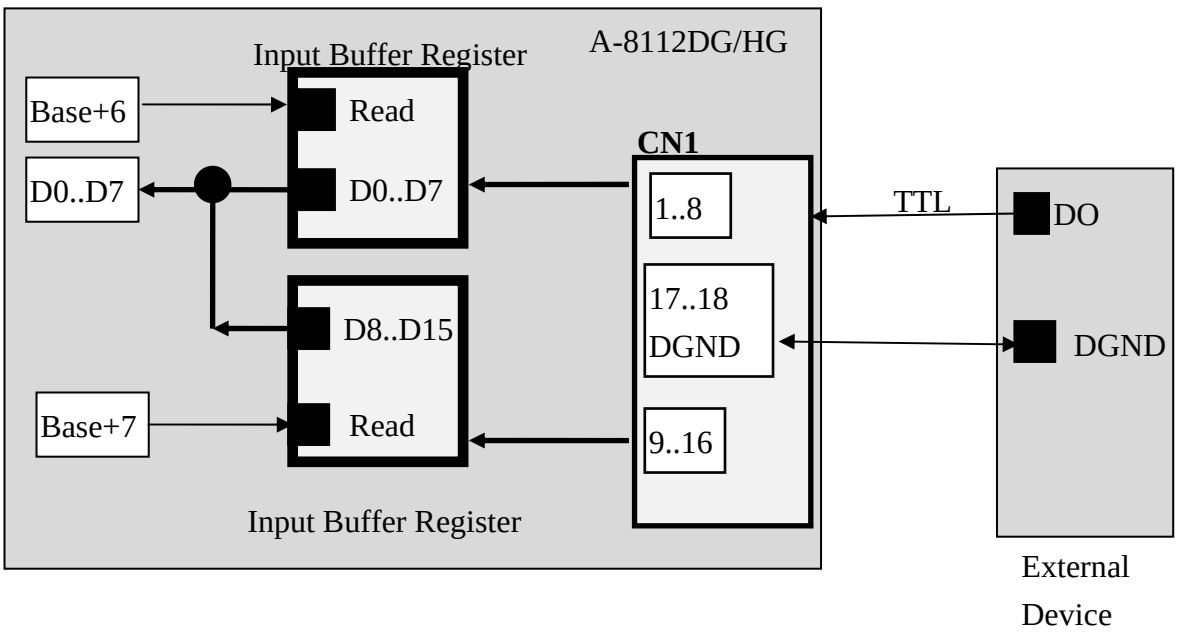
D/O 16 bits output data : D15..D0, D15=MSB, D0=LSB

The A-8112DG/HG provides 16 TTL compatible digital outputs. The low 8 bits are stored in address **BASE+D.** The high 8 bits are stored in address **BASE+E**

2.5 Digital I/O

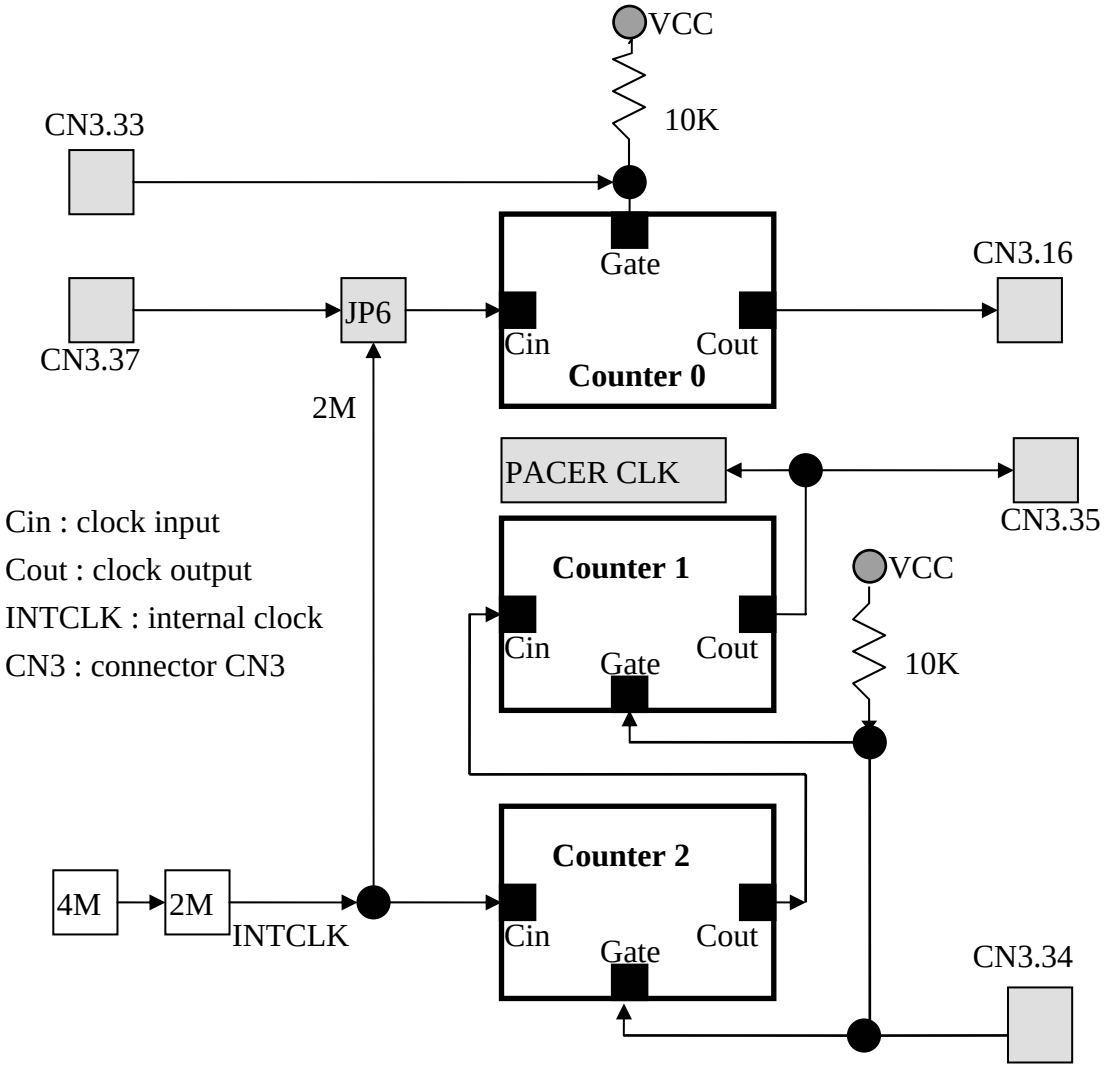
The A-8112DG/HG provides 16 digital input channels and 16 digital output channels. All levels are TTL compatible. The connections diagram and block diagram are given below:





2.6 8254 Timer/Counter

The 8254 Programmable timer/counter has 4 resgisters from Base+0 through Base+3. For detailed programming information about 8254, please refer to Intel‘s “Microsystem Components Handbook”.The block diagram is as below.



The counter0, counter1 and counter2 are all 16 bits counter. The counter 1 and counter 2 are cascaded as a 32 bits timer. This 32 bits timer is used as **pacer timer**. **The software driver, A822_Delay(), use counter 0 to implement a machine independent timer for settling time delay (sec. 2.4.6 and sec. 2.4.7).** If user doesn’t use A822_Delay(), the counter0 can be used as a general purpose timer/counter.

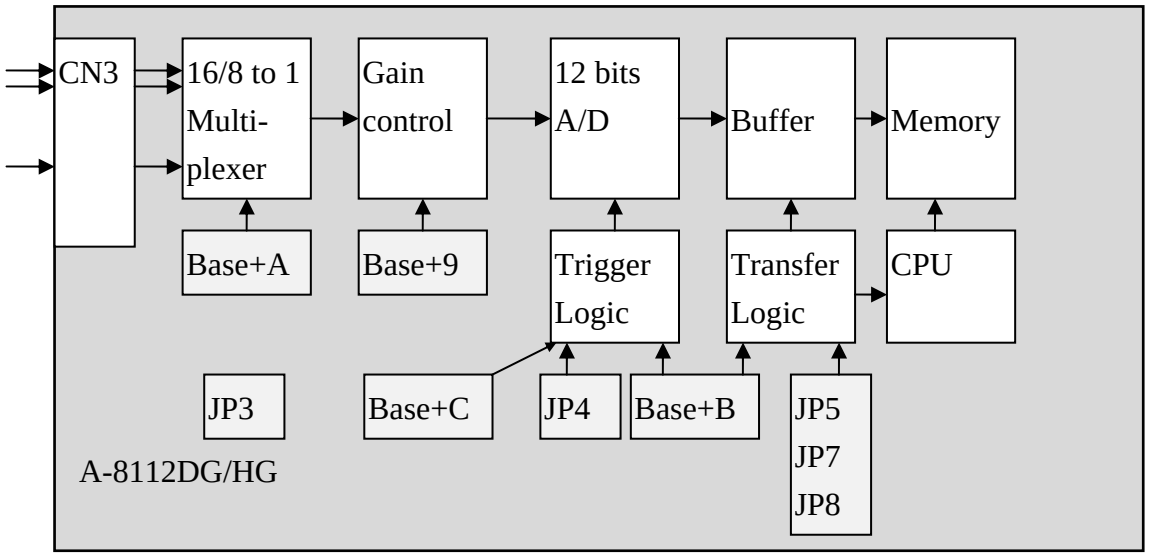
NOTE : When user call A822_Delay() to implement a machine independent timer, the JP6 must select internal 2M clock.

2.7 A/D Conversion

This section explains how to use A/D conversions. The A/D conversion can be triggered in any of 3 ways, **by software trigger, by pacer trigger or by external trigger** to the A/D converter. At the end of A/D conversion, it is possible to transfer data by any of 3 ways; those are **polling, interrupt and DMA.** Before use the A/D conversion function, user should notice the following issue:

- A/D data register, BASE+4/BASE+5, store the A/D conversion data **(sec. 2.4.2)**
- A/D gain control register, BASE+9, select gain **(sec. 2.4.6)**
- A/D multiplex control register, BASE+A, select analog input **(sec. 2.4.7)**
- A/D mode control register, BASE+B, select trigger type and transfer type **(sec. 2.4.8)**
- A/D software trigger control register, BASE+C **(sec. 2.4.9)**
- JP3 select single-ended **(sec. 2.3.3)**
- JP4 select internal/external trigger **(sec. 2.3.4)**
- JP5 select IRQ level **(sec. 2.3.5)**
- JP6 select internal/external clock for counter0 **(sec. 2.3.6)**
- JP7,JP8 select DMA channel **(sec. 2.3.7)**
- **3 trigger logic : software, pacer, external trigger (sec. 2.4.8)**
- **3 transfer logic : polling, interrupt, DMA (sec. 2.4.8)**

The block diagram is given below:



2.7.1 A/D conversion flow

Before using the A/D converter, the user should setup the following hardware item:

1. select single-ended (JP3) **(refer to Sec. 2.9 first)**
2. select internal trigger or external trigger (JP4)
3. select IRQ level if needed (JP5)
4. select DMA channel if needed (JP7,JP8)
5. select internal clock or external clock for counter0 if needed (JP6)

Then the user must decide which A/D conversion mode will be used. The software driver supports three different modes: **polling, interrupt and DMA.** The user can control the A/D conversion by polling mode very easy (sec. 2.4.9). It is recommended to use the software driver if using interrupt or DMA mode.

The settling time of multiplexer depends on the source resistance. Because the DOS driver **doesn't take care of the settling time**, **the user should delay enough settling time if switching from one channel to next channel. (sec. 2.4.7)**

The gain control module also need settling time if gain control code changed. Because the software **doesn't take care the settling time**, **the user should delay enough settling time if gain control code changed. (sec. 2.4.6)**

The software driver provides **a machine independent timer, A822_Delay()**, for settling time delay. This subroutine assume that JP6 select internal 2M clock and use counter0 to implement a machine independent timer. If the user call A822_delay(), the counter0 will be reserved and can't be used as a user programmable timer/counter.

The output of gain control module feed into the A/D converter. **The A/D converter needs a trigger signal to start an A/D conversion cycle**. The A-8112DG/HG supports three trigger mode, **software, pacer and external trigger**. The result of A/D conversion can be transfer into CPU by three modes: **polling, interrupt and DMA**. The operation mode is introduced in **sec. 2.4.8.**

2.7.2 A/D Conversion Trigger Modes

A-8112DG/HG supports three trigger modes.

1 : Software Trigger :

Write any value to A/D software trigger control register, BASE+A, will initiate an A/D conversion cycle. This mode is very simple but very difficult to control sampling rate.

2 : Pacer Trigger Mode :

The block diagram of pacer timer is show in section 2.6. The pacer timer can give very precise sampling rate.

3 : External Trigger Mode :

When a rising edge of external trigger signal is applied, an A/D conversion will be performed. The external trigger source comes from pin 17 of CN3.

2.7.3 A/D Transfer Modes

A-8112DG/HG supports three transfer modes.

1 : polling transfer :

This mode can be used with all trigger modes. The detail information is given in section 2.4.8. The software scans A/D high byte data register, BASE+5, until BUSY_BIT=0.The low byte data is also ready in BASE+4.

2 : interrupt transfer :

This mode can be used with pacer trigger or external trigger. The detail information is given in section 2.4.8.The user can set the IRQ level by adjusting JP5. A hardware interrupt signal is sent to the PC when an A/D conversion is completed.

3 : DMA transfer :

This mode can be used with pacer trigger or external trigger. The detail information is given in section 2.4.8. The user can set the DMA channel by adjusting JP7, JP8. Two hardware DMA requests signal are sent sequentially to the PC when an A/D conversion is completed. The single mode transfer of 8237 is suggested.

If using interrupt or DMA transfer, it is recommended to use A-822 software driver.

2.7.4 Using software trigger and polling transfer

If user needs to direct control the A/D converter without the A-8112 software driver. It is recommended to use software trigger and polling transfer. The program steps are listing as below:

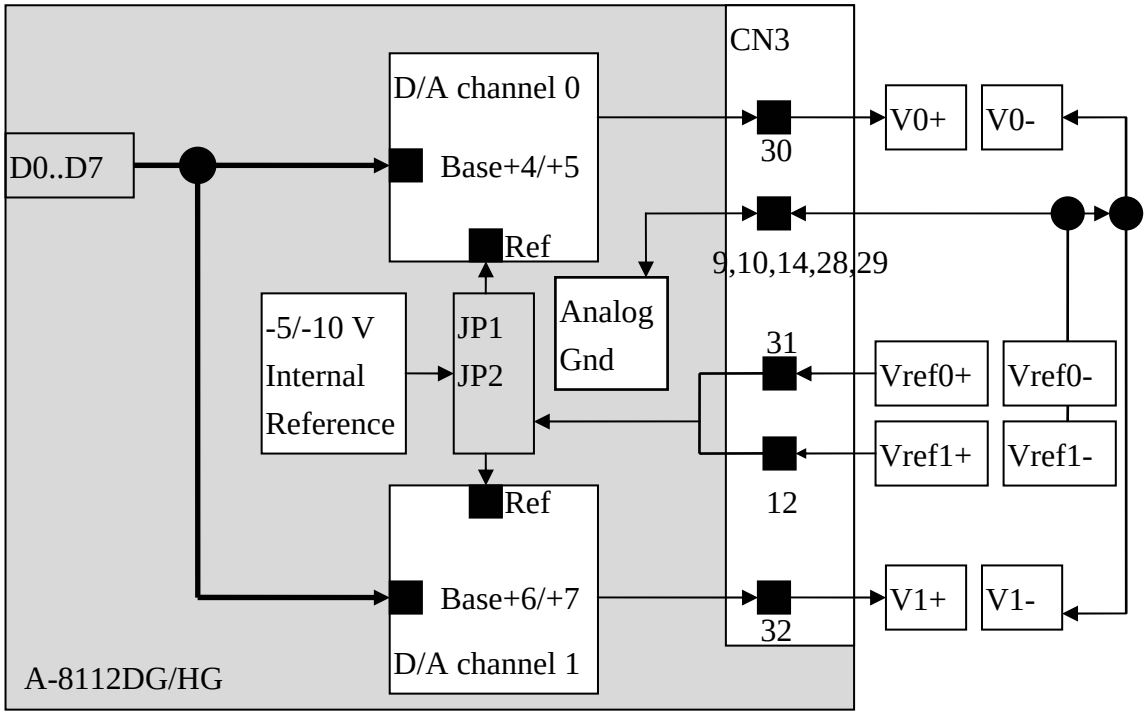
1. send 0x01 to A/D mode control register (software trigger + polling transfer) **(refer to Sec. 2.4.8)**
2. send channel number to multiplexer control register **(refer to Sec. 2.4.7**)
3. send the gain control code value to gain control register **(refer to Sec 2.4.6)**
4. delay the settling time **(refer to Sec. 2.4.6 and Sec. 2.4.7)**
5. send any value to software trigger control register to generate a software rigger signal **(refer to Sec. 2.4.9)**
6. scan the BUSY bit of the A/D high byte data until BUSY=0 **(refer to Sec. 2.4.2)**
7. read the 12 bits A/D data **(refer to Sec. 2.4.2)**
8. convert this 12 bits binary data to the floating point value

2.8 D/A Conversion

The A-8112DG/HG provides two 12 bits D/A converters. Before using the D/A conversion function, user should notice the following issue:

- D/A output register, BASE+4/BASE+5/BASE+6/BASE+7, (sec. 2.4.3)
- JP1 select internal reference voltage -5V/-10V (sec. 2.3.1)
- JP2 select internal/external reference voltage (sec. 2.3.2)
- If JP2 select internal and JP1 select -5V, the D/A output range from 0 to 5V
- If JP2 select internal and JP1 select -10V, the D/A output range from 0 to 10V
- If JP2 select external, the external reference voltage can be AC/DC +/- 10V

The block diagram is given as below:



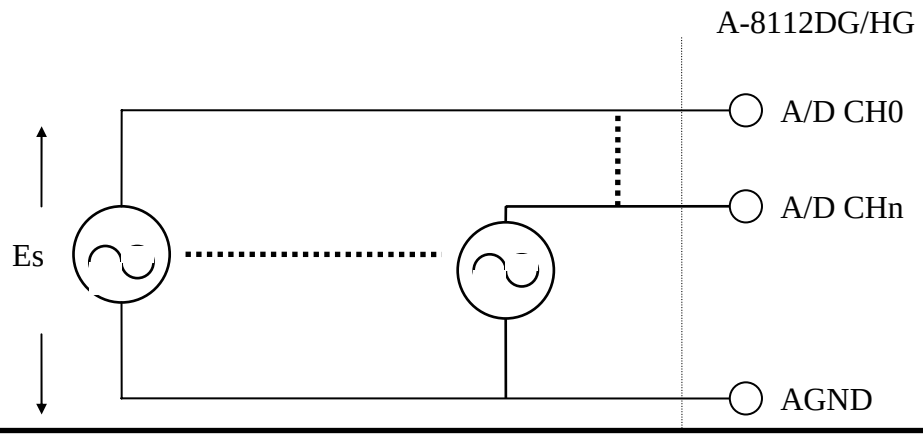
NOTE : The DA output latch registers are designed as "double buffer" structure. **The user must send the low byte data first, then send the high byte data to store the DA 12 bits digital data**. If the user only sends the high byte data, then the low byte data will be still the previous value. Also if the user send high byte first then send low byte, the low byte data of DA are still hold in the previous one.

2.9 Analog Input Signal Connection

The A-8112DG/HG is used to measure single-ended type analog input signal. Some analog signal can be measured in both of single-end or differential mode but some only can be measured in one of the single-ended or differential mode. With using A-8112, users have to make sure the analog signal is suitable with single-ended mode measurement.

The single-ended analog signal connection method is shown in Fig1.

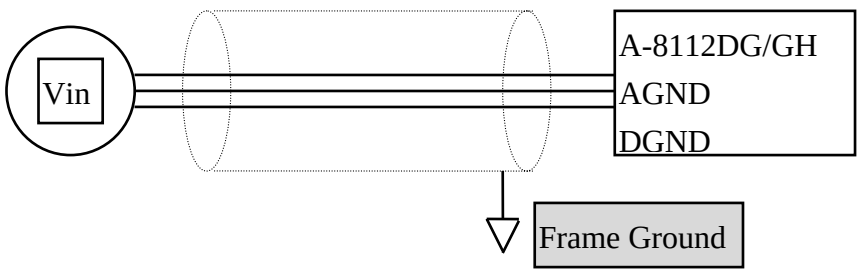
Fig1 : Connecting to singled-ended input configuration



Note : In Fig1, the maximum common mode voltage between the analog input source and the AGND is 70Vp-p, so the user must make sure that the input signal is under specification first. If the common mode voltage is over 70Vp-p, the input multiplexer will be damaged forever.

Signal Shielding

- Signal shielding connections in Fig1
- Use single-point connection to **frame ground (not AGND or DGND)**



2.10 Using DB-8225 CJC Output

The DB-8225 daughter board built-in CJC Circuitry is provided producing 10mV per Deg C With 0.0 Volts @ -273 Deg C. The A-8112 should be protected from draughts and direct sunlight in order to accurately reflect room temperature.

CJC Calibration:

1. Connect the A-8112DG/HG to DB-8225 CN1
2. Make sure A-8112DG/HG is at Single-ended Mode
3. Set JP1 to 1-2 and JP2 to 2-3 (Single-ended mode on DB-8225)
4. Read the temperature from a digital thermometer placed near D1/D2(See DB-8225 Layout) .
5. Read A-8112DG/GG analog input channel 0 (single-ended Channel 0)
6. Adjust VR1 until a stable reading of 10mV per deg C is attained.

For example, when the environment temperature is 24 deg C. the reading value of CJC will be 2.97V

(273 deg c +24 deg c) X 10 mV/deg c = 2.97V

You need an A/D Channel for CJC calibration. AI0 is reserved for CJC calibration use in single ended mode.

3. Connector

The A-8112DG/HG provides three connectors: Connector 1, **CN1, function as 16 bits digital input.** Connector 2, **CN2, function as 16 digital output**. Connector 3, **CN3, function as analog input, analog output or timer/counter input/output**.

3.1 CN1/CN2/CN3 Pin Assignment

CN1 : Digital Input Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Digital Input 0/TTL	2	Digital Input 1/TTL
3	Digital Input 2/TTL	4	Digital Input 3/TTL
5	Digital Input 4/TTL	6	Digital Input 5/TTL
7	Digital Input 6/TTL	8	Digital Input 7/TTL
9	Digital Input 8/TTL	10	Digital Input 9/TTL
11	Digital Input 10/TTL	12	Digital Input 11/TTL
13	Digital Input 12/TTL	14	Digital Input 13/TTL
15	Digital Input 14/TTL	16	Digital Input 15/TTL
17	PCB‘s GND output	18	PCB‘s GND output
19	PCB‘s +5V output	20	PCB ‘s +12V output

CN2 : Digital Output Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Digital Output 0/TTL	2	Digital Output 1/TTL
3	Digital Output 2/TTL	4	Digital Output 3/TTL
5	Digital Output 4/TTL	6	Digital Output 5/TTL
7	Digital Output 6/TTL	8	Digital Output 7/TTL
9	Digital Output 8/TTL	10	Digital Output 9/TTL
11	Digital Output 10/TTL	12	Digital Output 11/TTL
13	Digital Output 12/TTL	14	Digital Output 13TL
15	Digital Output 14/TTL	16	Digital Output 15/TTL
17	PCB‘s GND output	18	PCB‘s GND output
19	PCB‘s +5V output	20	PCB‘s +12V output

CN3 : Analog input/Analog output/Timer/Counter Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Analog Input 0/+	20	Analog Input 8/+
2	Analog Input 1/+	21	Analog Input 9/+
3	Analog Input 2/+	22	Analog Input 10/+
4	Analog Input 3/+	23	Analog Input 11/+
5	Analog Input 4/+	24	Analog Input 12/+
6	Analog Input 5/+	25	Analog Input 13/+
7	Analog Input 6/+	26	Analog Input 14/+
8	Analog Input 7/+	27	Analog Input 15/+
9	PCB‘s analog GND output	28	PCB‘s analog GND output
10	PCB‘s analog GND output	29	PCB‘s analog GND output
11	D/A‘s internal -5V/-10V voltage reference output	30	D/A channel 0‘s analog voltage output
12	D/A channel 1‘s external voltage reference input	31	D/A channel 0‘s external voltage reference input
13	PCB‘s +12V output	32	D/A channel 1‘s analog voltage output
14	PCB‘s analog GND output	33	User timer/counter‘s GATE control input
15	PCB‘s digital GND output	34	Timer/counter 1&2‘s GATE control input
16	User timer/counter‘s output	35	Timer/counter 1‘s output
17	External trigger source input/TTL	36	Reserved
18	Reserved	37	User timer/counter‘s external clock input (internal=2M)
19	PCB‘s +5V output	XXXXXXX	This pin not available

3.2 Daughter Board

The A-8112DG/HG can be connected with many different daughter boards. The function of these daughter boards are described as follows.

3.2.1 DB-8225

The DB-8225 (or ACLD-8125) provides a **on-board CJC**(Cold Junction Compensation) circuit for thermocouple measurement and **terminal block** for easy signal connection and measurement . The CJC is connected to A/D channel_0. The A-8112DG/HG can connect CN3 direct to DB-8225 through a 37-pin D-sub connector.

3.2.2 DB-37

The DB-37 (or ACLD-9137) is a **general purpose** 37-pin connector. This board directly connects to a 37-pin D-sub connector. It is suitable for easy signal connection and measurement.

3.2.3 DB-16P

The DB-16P (or 782 series) is a **16 channel isolated digital input** board. The A-8112DG/HG provides 16 channel non-isolated TTL-compatible digital inputs from CN1. If connecting to DB-16P, the A-8112DG/HG can provide 16 channels isolated digital input signals. Isolation can protect PC if abnormal input signal is occurred.

3.2.4 DB-16R

The DB-16R (or 785 series) provides **16 channel SPDT relay output.** The A-8112DG/HG provides 16 channel TTL-compatible digital output from CN2. If connecting to DB-16R, the A-8112DG/HG can provide 16 channel relay output to control power device.

4. Calibration VR Description

There are seven VRs on the A-8112DG/HG. Calibration need to adjust all seven VRs.

VR Num.	Description
VR1	A/D‘s offset adjustment
VR2	A/D‘s gain adjustment
VR3	D/A channel 0‘s gain adjustment
VR4	D/A channel 1‘s gain adjustment
VR5	D/A‘s reference voltage adjustment
VR6	A/D unipolar‘s offset adjustment
VR7	A/D programmable amplifier‘s offset adjustment